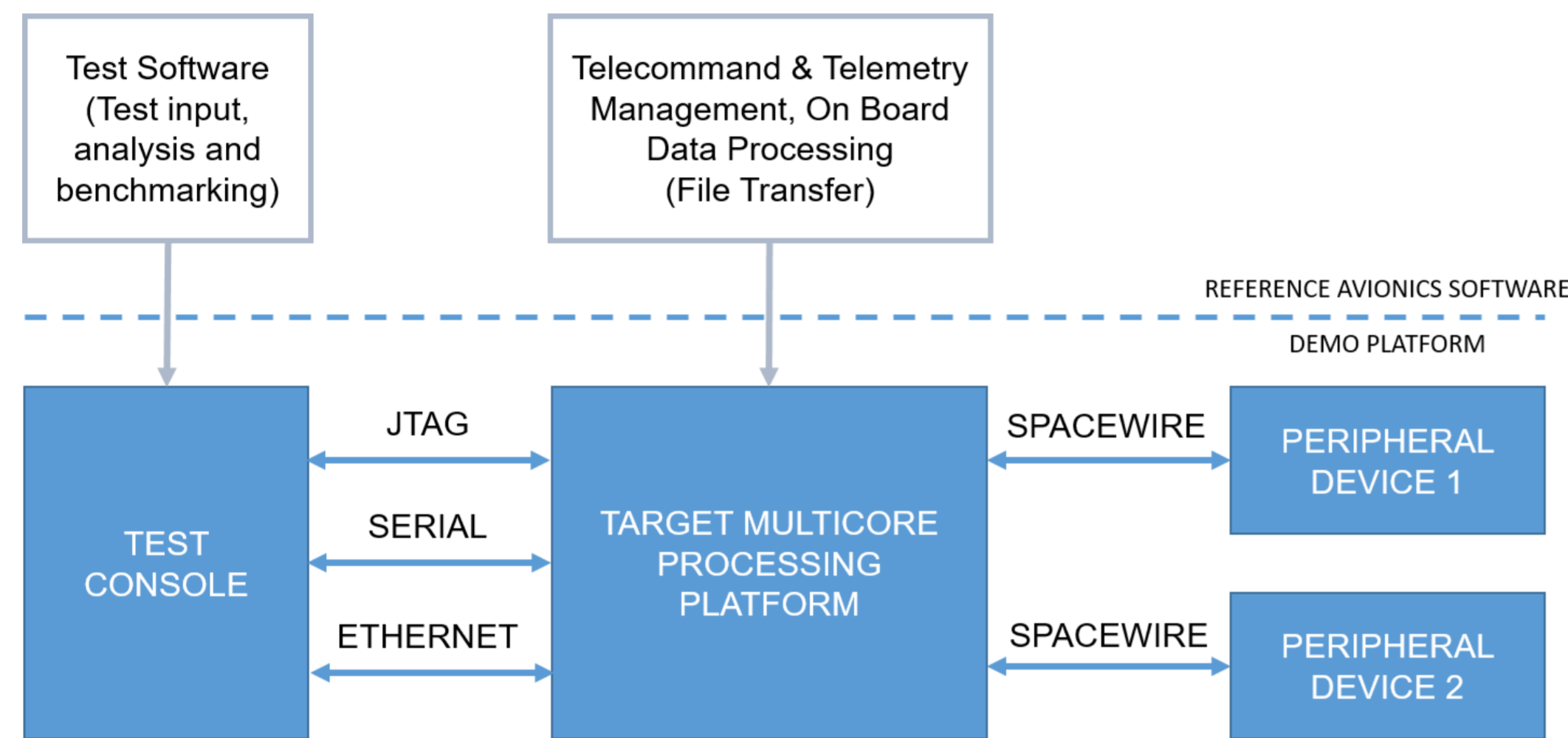


## Introduction

Multi-core architectures will be adopted in the next generations of avionics and aerospace systems. With the advent of Integrated Modular Avionics (IMA), these systems progressively became mixed-criticality systems, and spatial and temporal isolation is thus a key requirement. In such a context, virtualization appears to be a promising technique to implement robust software architectures in multi-core avionics platforms. Hence, this work explores the possibility of using virtualization in the definition of a multi-core test platform for the aerospace domain. This is a first attempt to exploit paravirtualization on Cobham-Gaisler LEON4, the European Space Agency next generation microprocessor.

## Reference Application

In the context of WP9 Task T9.4, TASI and Univaq are collaborating on the implementation of a reference Spacecraft Platform based on a next-generation multicore processing architecture.



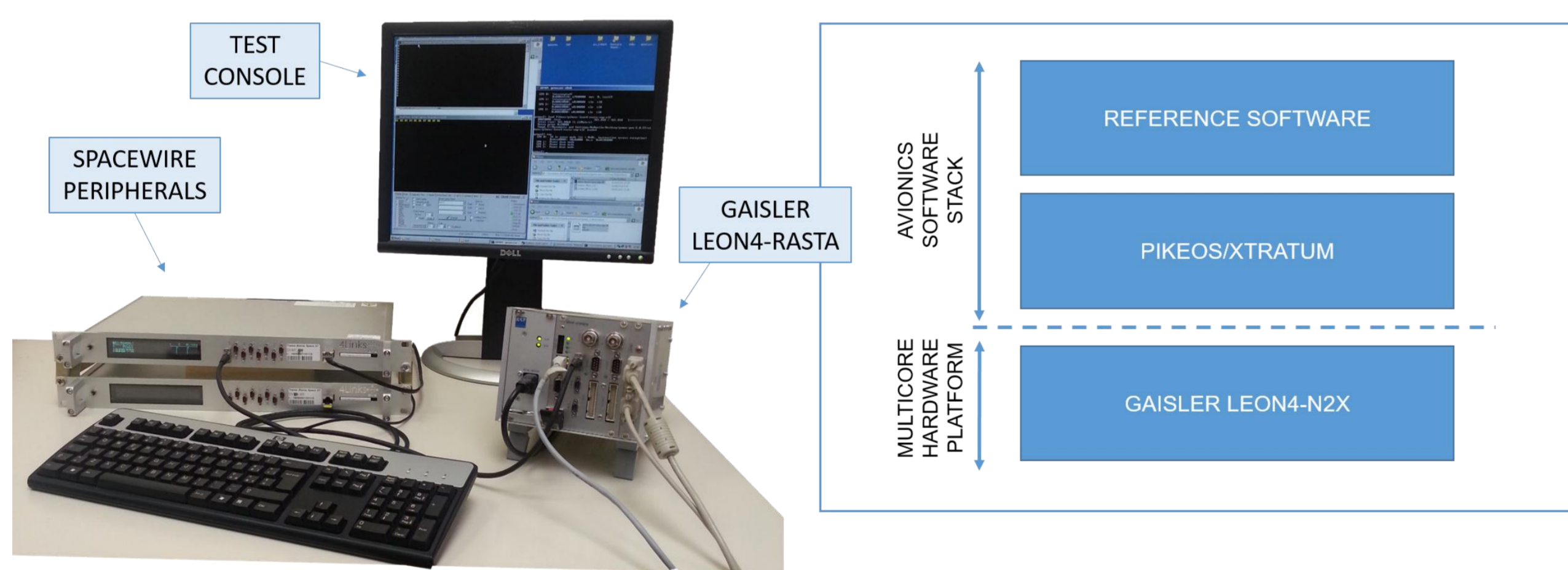
The platform management presents specific requirements of reliability, robustness, as well as various levels of criticality and dependability both at software and hardware level. The use of hypervisors and paravirtualization techniques is considered as a feasible way to deal with these requirements.

Overall objectives of Task T9.4:

- Implementation and analysis of a typical mixed-critical aerospace application over a next-gen multicore platform
- Assessment and analysis of virtualization technologies (isolation)
- Comparison of different hypervisors (robustness, self-healing)

## Platform & Tools

The target hardware identified by TASI and Univaq is a quad-core architecture based on the Gaisler SPARC-V8 LEON4 processor (ESA's Next Generation MicroProcessor).



Two different hypervisors, SYSGO PikeOS and FentISS XtratuM, have been considered for the implementation of the reference application on selected multicore platform.

- PikeOS is a platform providing RTOS, type I hypervisor and paravirtualization functionalities.
- XtratuM is an open-source, bare metal hypervisor targeting real-time systems and implementing the paravirtualization principle.

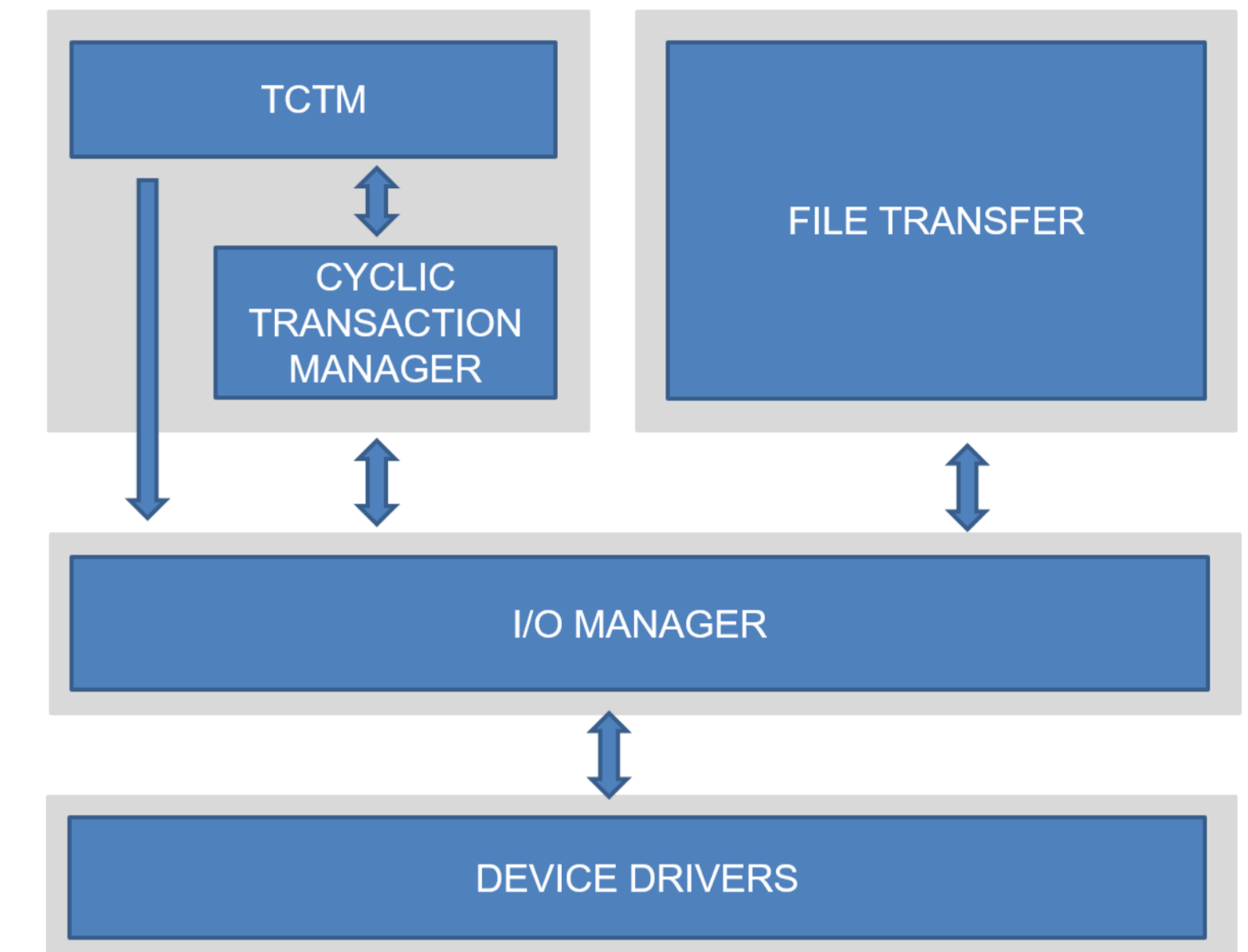
## Results and future work

- The infrastructure of proposed application has been defined. Different implementation strategies using both XtratuM and PikeOS have been analyzed.
- Both the hypervisors have been analyzed and benchmarked with respect the target multicore platform. Required dedicated software component have been implemented and tested.
- A first alpha release of the application has been recently finalized. The correct functionality of defined component has been verified.
- Proposed platform will be further extended in the near future, carefully assessing the performance of the system in relation to specific requirements of the aerospace domain.

## Software Architecture

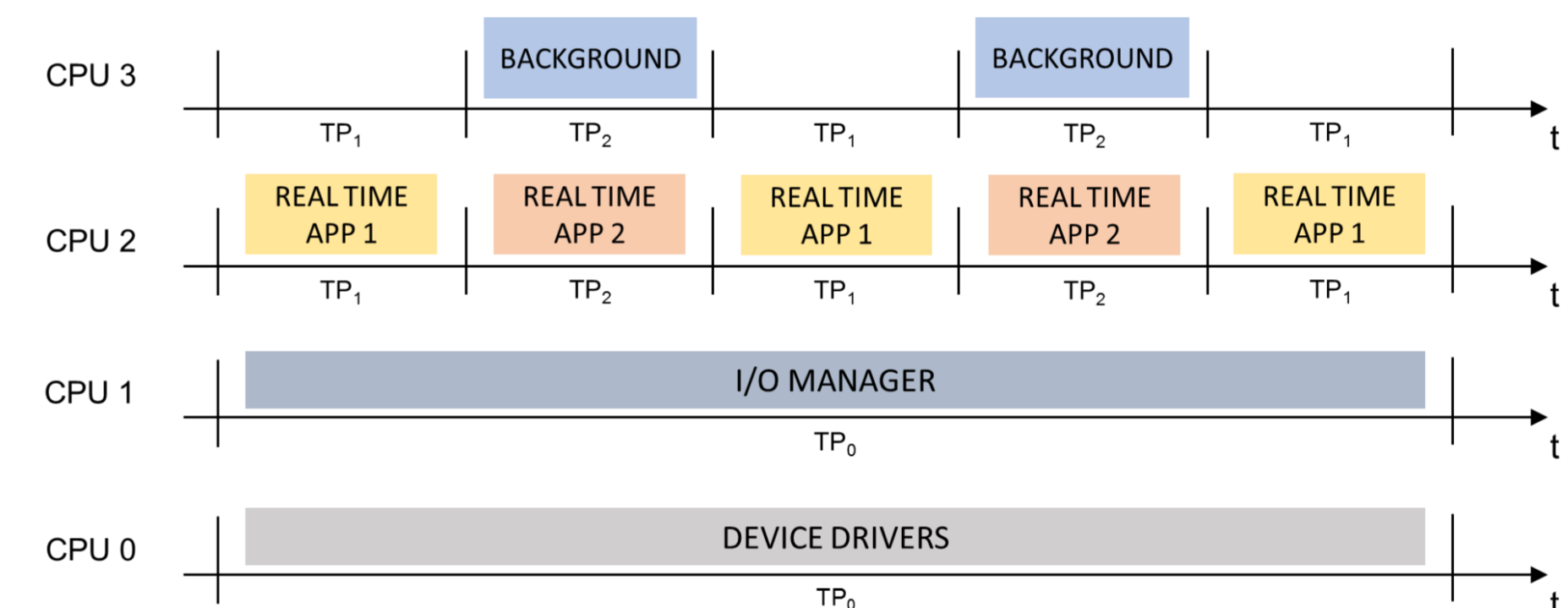
The avionics software architecture includes various components running on top of the hypervisor:

- Applications: TCTM, File Transfer
- Cyclic Transaction Manager: packet formatting
- I/O Manager: low level management of data transactions
- Device Drivers: UART, SpaceWire, Ethernet



## Time and Space Partitioning

Defined software objects have been mapped to separate partitions. The allocation of partitions to different CPUs has been then analyzed, specifically considering functional and timing requirements.



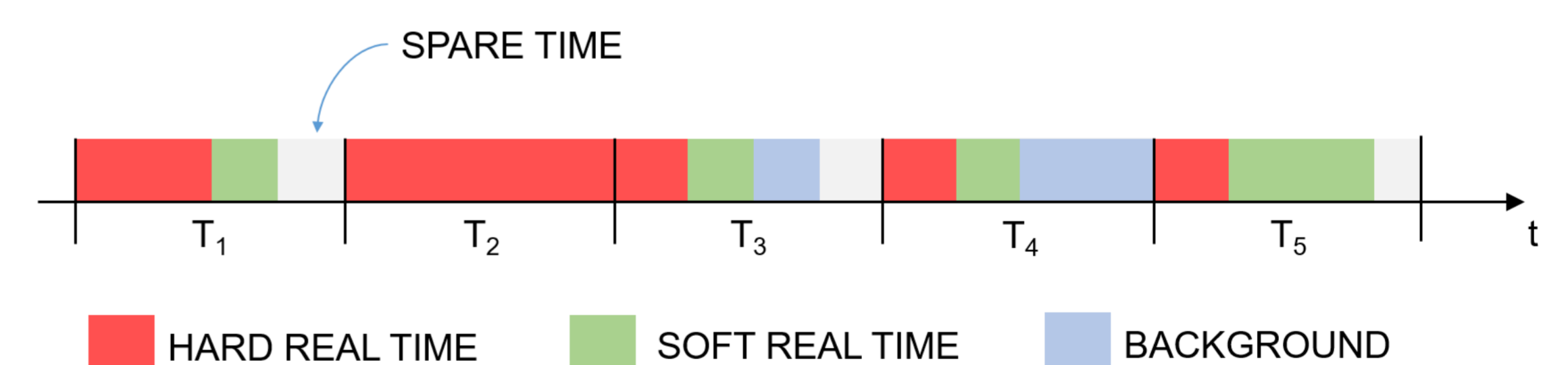
Specific focus has been put in the design of the I/O manager component:

- Mapping of different types on transactions (Cyclic and Sporadic TCTM transactions, File transfers) on different traffic classes
- Definition of scheduling rules for an efficient traffic management

## I/O Management

Three different types of I/O transactions have been identified with respect to the timing requirements of the application tasks:

- Hard real-time transactions (TCTM)
- Soft real-time transactions (TCTM)
- Background transactions (file transfers)



The I/O Manager guarantees the satisfaction of the real time requirements and exploits the hypervisor services to deal with problematic situations.

## Contributing Partners: