

# ARTEMIS Technology Conference 2016

## EMC<sup>2</sup>

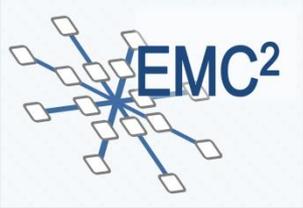
### Industrial manufacturing and logistics

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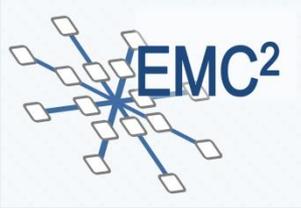
# Living laboratories and industry

## Four use cases



- What are these laboratories trying out
  - Combining hard and soft real time functions on a multicore
  - Unique approach to provision of safety
  - Hybrid solutions for flexible roots of trust
  - Novel manufacturing quality control
  
- Starting point
  - Separate processors for hard real time tasks
  - Multiple physical components bound development time for safety
  - Single core solutions for secure elements
  
- What key methods will be used to achieve the results?
  - New architectures utilizing multicore chips are developed
  - Relevant results from technical work packages are adopted
  - Demonstrator are built and analyzed

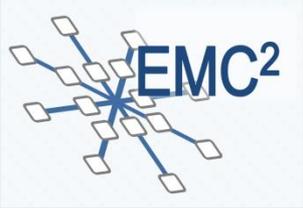
**AMBAR, BUT, Danfoss, DTU, FhG, ITI, LERO, NXP, UTRC**



# Use case 1: Drives and electric motors in industrial applications



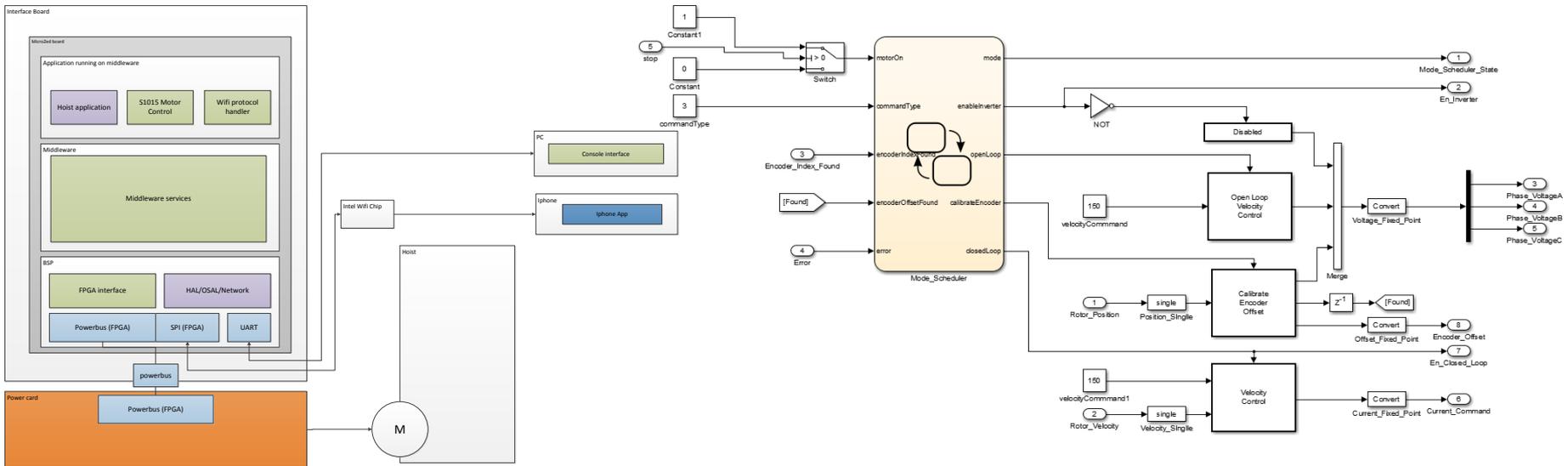
- Conceptual architecture addressing the requirements
  - Real time operation and design mixing real time and less critical operations
  - Development and study of model driven design covering automatic code generation and FPGA programming
  - Support for functional safety
- Two different prototypes have been developed
  - A prototype was demonstrating wide scale use of model driven development.
  - A prototype demonstrating mixed time domains and model driven motor control. Also functional safety concept was demonstrated.
- The prototypes were analyzed. The remaining gap between the results and the requirements will be used in improving the architectures.

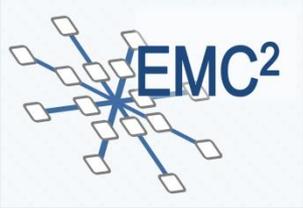


# Architectures



- Architecture that demonstrates that multi-core processors can be used to launch different control levels on different cores and FPGA with respect to criticality and safety aspects
- Predictability solution related to WP3, prepared to use OSSS-MC technology from WP2, tool support for FPGA SW development based on WP2, safety evaluation planning to adopt OSLC solutions from WP6
- Model based design on both FPGA and  $\mu\text{P}$  demonstrated by UTRC

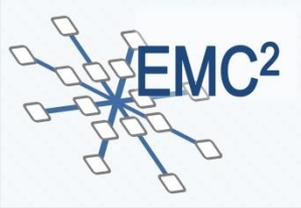




## Use case 2 – Identification and authentication



- Development of flexible multi-core root of trust
  - ensure strong security for sensitive data
  - fulfil increased performance requirements
  - provide interoperability for other system components
- Working prototype using commercially available off the shelf components was built to demonstrate the concept of a multi-core root of trust of module for any network
- After the core-functionality was tested using COTS components, a complete demonstrable system has been designed. The functionalities are tested with the help of a test bench that simulates host-client security requests.

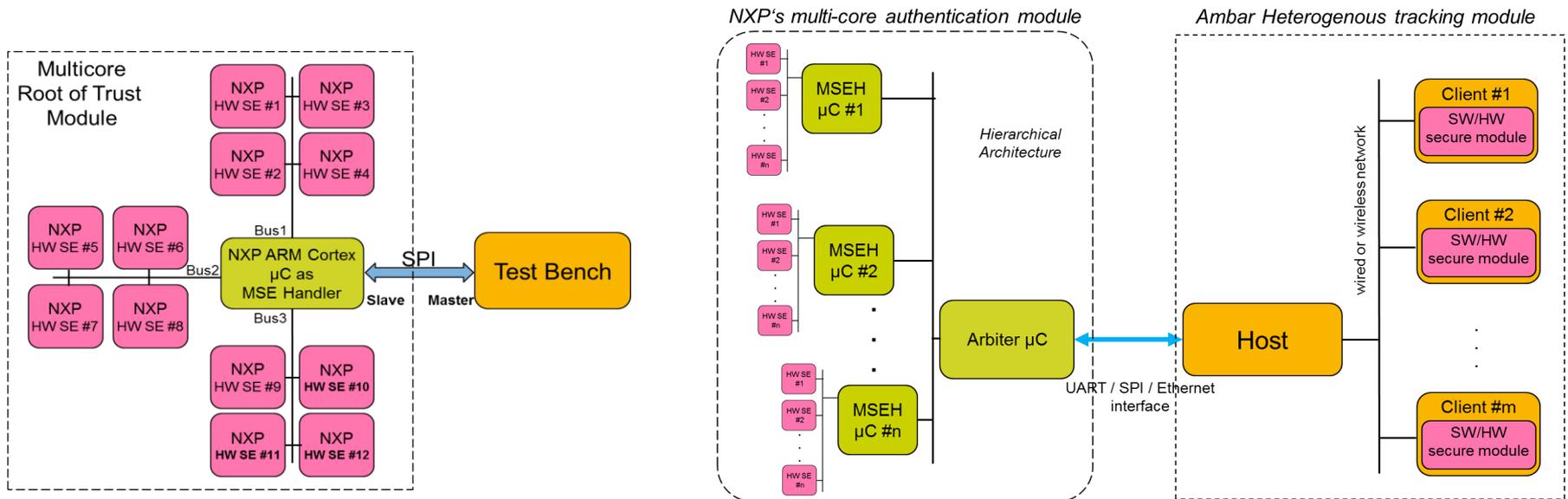


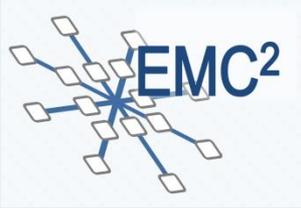
# Use case 2

## Design of the first prototype



- MSE Handler: Generic microcontroller interfacing multiple secure elements to test bench scheduling asynchronous security request from the networked clients.
- Secure element: Certified controller supporting authentication, encryption/decryption, digital signatures, certificates and secure storage with true random number generator.
- Test bench: Creates multiple client requests and simulates different load scenarios.

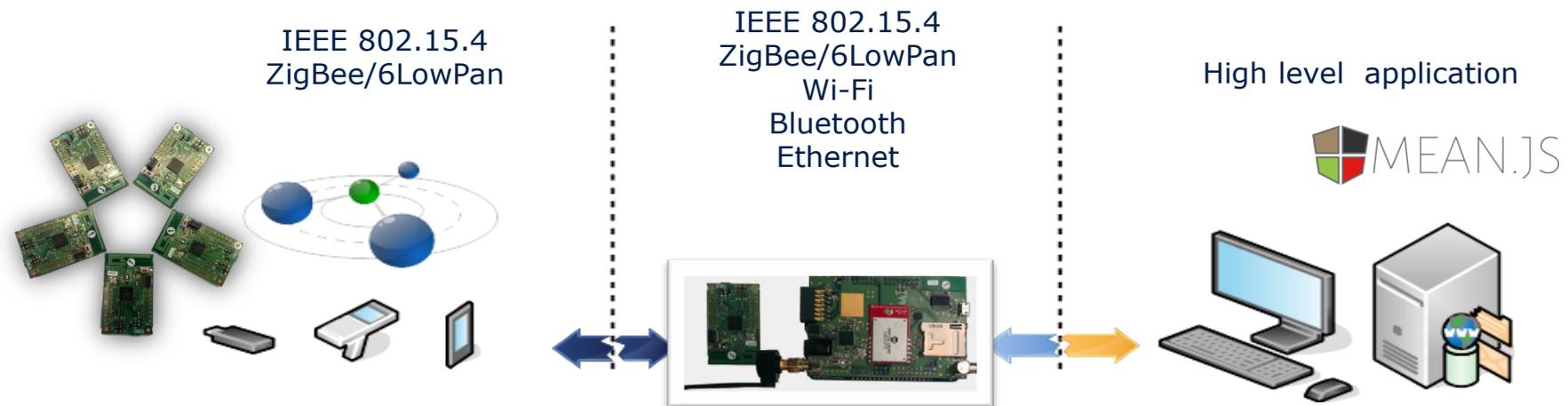


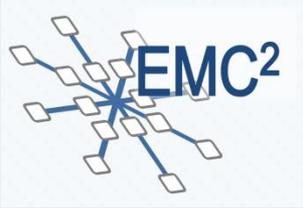


# Use case 3 - Tracking System Design



- Tracking functionality based on three subsystems:
  - **Tracking devices** based on multiple RF technologies for identification, location and monitoring.
  - **Concentrator** based on an embedded multi-core gateway that provides multi-standard communications (Wi-Fi, ZigBee/6LowPan, Bluetooth)
  - **Central server** based on web application technologies
- Communication stacks from WP3, custom console and IDE tools from WP5, integration with WP10 T2 to add security, design shared with T11.3 partners for home environments



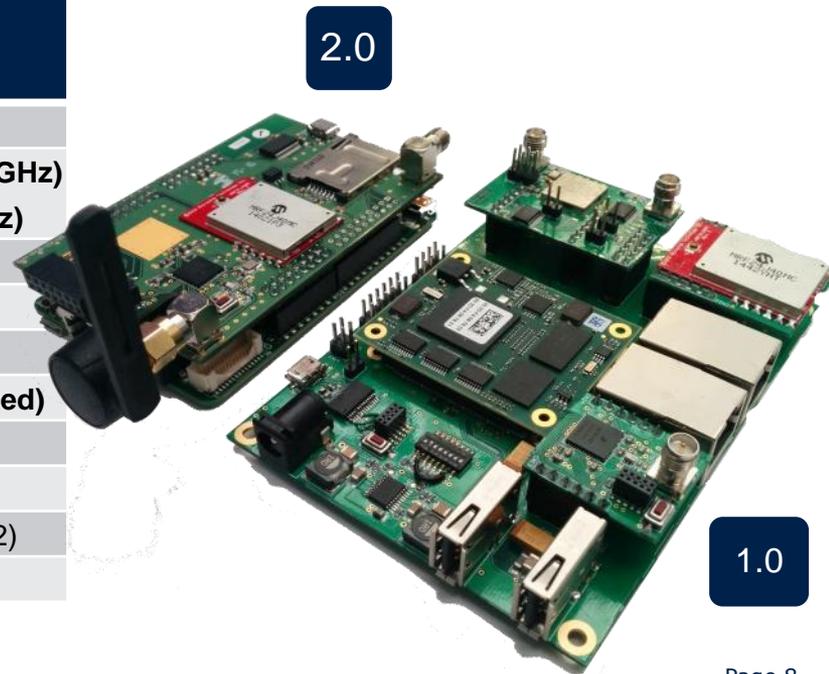


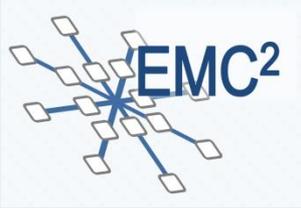
# Use case 3 - Tracking Design of the Gateway



- Design and implement the **embedded gateway** and **wireless nodes** that will serve as foundation of the tracking system.
- Integration of several wireless technologies: ZigBee/6LowPan, Wi-Fi, BLE, 3G and customization of the firmware.
- First prototype: Based on the **Vybrid** platform
- Second prototype: Based on **i.MX 6SoloX** platform
  - Improving form factor, performance, integration Wi-Fi/BLE

	GATEWAY Version 1.0	GATEWAY Version 2.0
Dimensions	115x85mm	90x60mm
Microprocessor	Multicore: Cortex-A5 (533 MHz) + Cortex-M4 (167 MHz)	<b>Multicore: Cortex-A9 (1GHz) + Cortex-M4 (200 MHz)</b>
OS	Linux (Debian)	Linux (Ubuntu)
Interfaces	Ethernet	Ethernet
	Wi-Fi	<b>Wi-Fi (integrated)</b>
	Bluetooth 4.0	<b>Bluetooth 4.0 (integrated)</b>
	ZigBee/6LoWPAN	ZigBee/6LoWPAN
		<b>GSM/GPRS</b>
Power interface	USB/SPI/I2C/GPIO(x2) 5V/2A	USB/SPI/I2C/GPIO(x2) 12V/2A

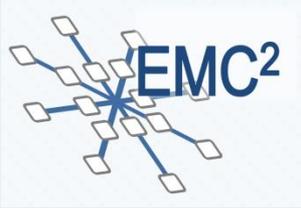




## Use case 4 - Manufacturing quality control by 3D inspection



- 3D inspection system based on a multi-camera configuration along a sphere-like structure that allows to observe the part under study angle without any occlusion
- Using set of captured images, the system reconstructs the 3D shape as well as texture of the object.
- This information is used to detect any significant deviation from the manufacturing parameters.
- A conceptual design and a prototype showing that through parallelization high enough performance can be achieved.
- Source code rewriting for algorithm intra-node parallelization has been developed. Sequential and a parallel model has been compared and modelled with the "art2kitekt" (WP 2).
- OpenMP parallelization improves response time around 3 times (24.563 milliseconds to 7.996 milliseconds).

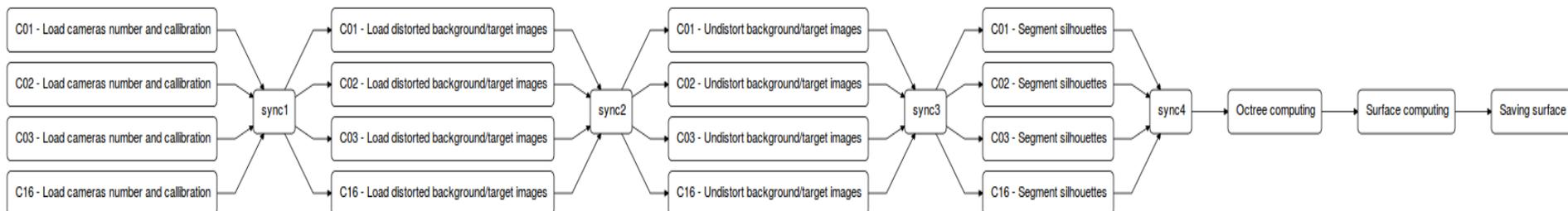
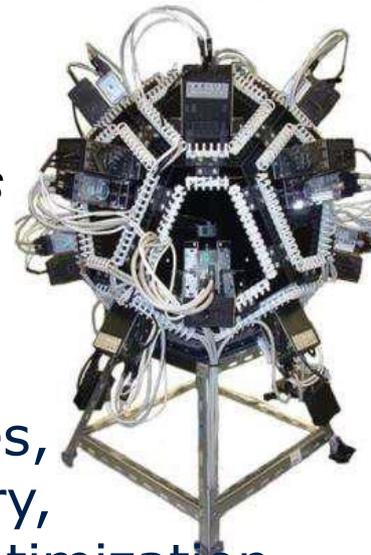


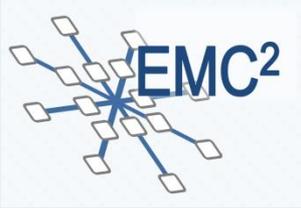
# Use case 4

## Prototype conceptual architecture



- In parallel
  - *calibration, background, undistort, segment silhouettes*
- Followed in sequence
  - *octree, surface and saving*
- Development using tools from technical WPs
  - WP2 tool *Pareon* to find invalid memory accesses, uninitialized memory reads, use of freed memory, race conditions, deadlocks, memory leaks) + optimization
  - WP6 tool *Vitro* has been used to generate a dataset (composed of springs, angles, screws and tubes)
  - WP2 tool *art2kitekt* used to represent and analyze the set of sequential and parallel tasks of the 3D reconstruction





# Summary



- The four use cases represent four different industrial applications that highlight wide range of different requirements and serve as laboratory for different technologies:
  - Variable Speed Drives in Industrial Applications is a complex active component in interaction with the physical environment, built with restricted operational resources, and operating reliably and safely under hard real-time constraints.
  - Identification and Authentication requires a solution that simultaneously ensure strong security for sensitive data, fulfill increased performance requirements, and provide enhanced interoperability for other system components.
  - In tracking the main challenge is to gather and process the location information in heterogeneous wireless networks while maintaining low system complexity and low costs. Tracking serves also as test bench for identification and authentication.
  - Manufacturing Quality Control by 3D Inspection places hard synchronization and capacity requirements before industrial inspection field can get an efficient and scalable solution to current technical challenges.
- We have made promising progress in all these fields and provided feedback for the technical work packages. Some of these results can later turn into products.