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EMC²
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WP4 HW Architectures & Concepts

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Activities bundled across 5 Technology Lanes:
Mixed Criticality Workshop
EMC2-WP4 – Technical Overview

Diagram of a system with various components and connections, including:
- External Memory Controller
- Configurable redundancy controller/checker
- HPS CPU
- LP CPU
- DSP CPU
- Multi-purpose memory blocks

Various labels for components and connections, such as:
- Tecnalia
- IFAT
- TUBS
- IFAG
- Sundance
- Chalmers
- UoBr
- AVL
- SevenSols
- TUD
- NXP DE
- TASE
- NXP NL
Mixed Criticality Workshop
EMC2-WP4 – Objectives / Highlights

➢ USPs/Highlights of WP4
  ▪ Architecture and Hardware support for mixed-criticality applications on multi-core platform along the 5 technology lanes
    ▪ EMC2-DP platform – Reconfiguration (T4.4)
    ▪ Software Defined Asymmetric Multiprocessing on EMC2-DP ZYNQ platform – Architecture(T4.2)
    ▪ Heterogeneous TTNoC many-core architecture – Networking (T4.3)
    ▪ High-Accurate Distributed Control Systems – Networking (T4.3)
    ▪ Analog-Mixed-Signal Power System for MC Multi-Core - Architecture
    ▪ System optimisation for MCMC applications
      ▪ Time-of-Flight 3D Imaging – Application & Demonstration (T4.6)
      ▪ Application-specific Exploration and Optimization MCMC Hardware with Virtual Hardware platform – Virtualization

➢ Status at start of period 3:
  ➢ Hardware platforms and tools applied to internal use-cases
  ➢ Ongoing evaluation and knowledge transfer of the proposed technologies and tools with other WPs and Living Labs
WP4 Achievements per technology
Analog-Mixed-Signal Power System (Infineon)

- First full functional safety compliant Analog-Mixed-Signal Power System for multi core and mixed critical systems including standby controller, robust concept implementation, out of operating range functionality is now fully available for next generation of products.

- It introduces highest flexibility and have very efficient regulators with SMPS power optimization features, reverse back biasing and dynamic voltage scaling.

Block diagram of the concept
Heterogeneous TTNoC many-core architecture (TU Wien)

Objective: Building a deterministic heterogeneous architecture on Altera Arria V SoC

Key achievements:
- Integration of TTNoC on the Arria V SoC platform.
- The architecture combines 4 Nios 2 components and an ARM Cortex A9 component.
- Full time and space isolation of individual components, designed for mixed-criticality applications.
Software Defined Asymmetric Multiprocessing on EMC2-DP ZYNQ platform

- **EMC2-DP** is Sundance HW platform enabling to use System on Module Component with ZYNQ.

- **EMC2-DP** is compatible with the Xilinx Software Defined System on Chip (SDSoC 2015.4) flow. UTIA & Sundance designed support for SDSoC.

- **EMC2-DP** parameters: MicroBlaze and UTIA EdkDSP floating point accelerator deliver:
  - Adaptive LMS filter: 776 MFLOP/s

  - This is **2.3x faster** than 666 MHz ARM A9 CPU optimized SW with NEON vector proc. unit.

- **EMC2-DP** HW image processing accelerators are generated by the SDSoC from C. See figure: Edge detection on Full HD Video:
  - **EMC2-DP ARM + SDSoC HW**: 60.0 Frames/s
  - **EMC2-DP ARM + platform SW**: 5.3 Frames/s
High-Accurate Distributed Control Systems (SevenS)

- Development of new White Rabbit nodes for the project to improve scalability and stability of the distributed frequency:
  - White Rabbit ZEN
  - White Rabbit LEN

- In terms of time in distributed networks considered as critical data, we have adapted White-Rabbit (able to provide time with <1ns accuracy) and also using our own devices, two distribute time over 14 hops maintaining synchronization capabilities with a jitter in 1-PPS signal under 250ps

- A new clock distribution mechanism (Peer-to-Peer and PeerDelay) to provide White-Rabbit with the possibility of being adapted to industrial Ethernet networks, which opens doors to the development of redundancy protocols such as High-availability Seamless Redundancy (HSR).
Objective: Exploration of novel Time-of-Flight 3D imaging concepts targeting multi-cores and mixed-criticality

Key achievements

- ToF / RGB sensor fusion
  - First time high-performance sensor fusion solution for mobile devices achieved
  - Upscaled resolution, increased sharpness, less noise, less motion artifacts, high FPS

- HW-accel. ToF processing
  - Novel Zynq-based system solution for mixed-critical app.
Prototype A: <1ns accuracy deterministic time distribution system

Main features:
- **WR-ZEN** board as main time provider (better oscillator)
- **WR-LEN**, a double-port WR node
- **Accuracy <1ns** synchronization
- 1 Pulse per Second and 10MHz outputs
- Daisy-chain configurations with less than **250ps of jitter**
- **Scalable up to 12 nodes** in cascade
- Time distribution using **WR-PTP and IRIG-B**.
- Remote Time Units (RTU) connected to WR devices using IRIG-B

Prototype A
- Setup to demonstrate the scalability of the timing solution and also the utilization of different timing protocols in the same network.

Live-Demo available in Y2 Review

Legend:
- Optical Fiber (WR)
- Coaxial (IRIG-B, PPS,....)
- Serial (NMEA, TOD,....)
Prototype B: Single point of failure avoidance using Transparent Clocks (Redundancy Protocols)

Main features:

- <1ns synchronization
- 1 Pulse per Second (1-PPS) and 10MHz outputs
- **Redundancy Capabilities** (HSR implementation for timing)
- Able to **recover** from a link failure in ~zero-time.
- 1-PPS skew improvement in terms of ~50ps

Prototype B

- Implementation of the HSR redundancy protocol using Transparent Clocks to recover from a system failure in ~zero-time.
- Demo will consist in how two devices connected to a HSR ring are able to remain 1-ns synchronized even after the main time reference is lost (link down).

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Mixed Criticality Workshop
EMC2-WP 4 – Technology Transfer

Technology transfer phases

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Scope 1: Complete implementation into use cases in the project
Scope 2: Partial implementation into use case
Scope 3: Will be transferred to LL (WP7-12) but not implemented into use case
Scope 4: Topic for future applications; technology transfer subsequent to EMC2