Art2Kitekt A toolset to model and analyze mixed criticality, real-time systems Sergio Sáez, Vicent Castelló, Ismael Salvador, Rubén de Juan, Ken Sharman, Javier Cano

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Abstract

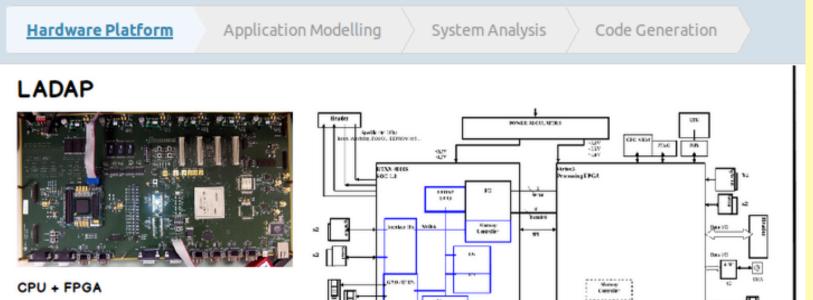
The target is to develop a **software tool suite** for the design of HW and SW of mixed criticalilty, real-time systems. Some remarkable points:

1) A set of **tools for helping the engineer** that has to analyse and design a highlyintegrity system. The target system is composed of HW and SW elements. Both SW and HW will be parameterized and represented by the tool.

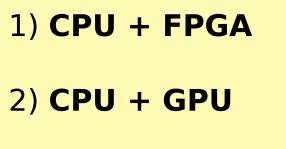
2) The tool will provide the most **elementary analysis and assistance, as well as other more advanced features** (offline analysis with complex algorithms to find the best plan).

Hardware Platform

Different **execution platforms predefined** and available for the engineer to configure with the corresponding parameters of the specific hardware that is going to be used .



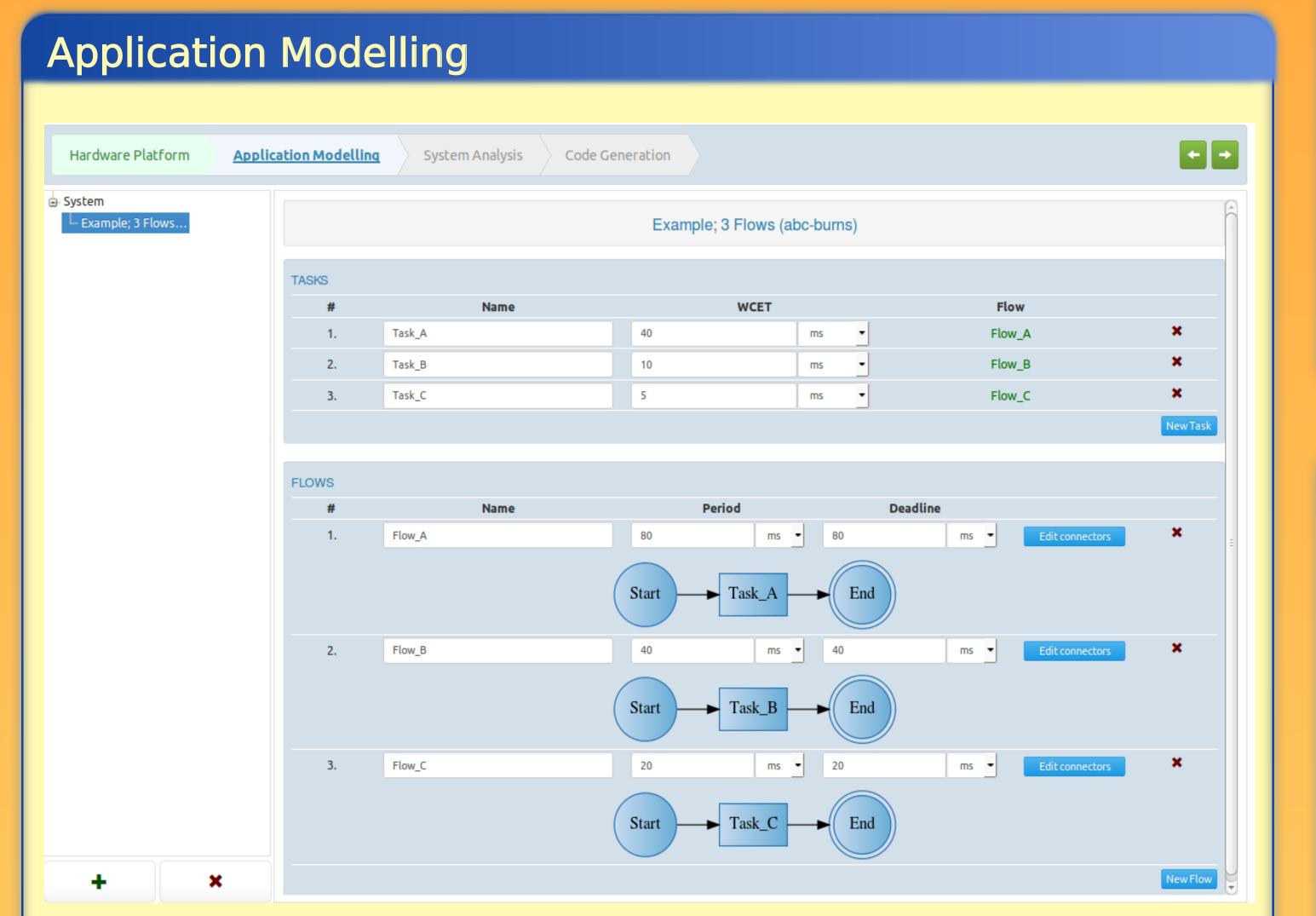
Currently, next platforms are planned to be defined:



3) **CPU + CPU**

3) The tool will automate a part of the design phase and generate evidences **to pass the certification process** of the highly-integrity systems designed.

4) The input of the tool will consist of a number of parameters from hardware platform and application models. The output will be a **cyclic task plan in both table and source code** (C languaje) formats.



RTAX-4000S (SOC L3) + VIRTEX 5		Comp Landy			
MEMORY	Name 🔺	State 🗧	BandWidth	Blocked Time	Latency
VIRTEX 5	SpWi/F #1			-	-
	SpWi/F #2	CONNECTED	100	Ø	23
SERIAL I/O BUSES	SpWi/F #3				
	SpWi/F #4				

4) **CPU + NoC + 2 DSP**

Each one of them is intended to be used with industrial partners to verify and take advantage of its functionality.

The engineer will be able to **custom the execution platform** in terms of CPUs, memories, buses, reconfigurable hardware, devices, operating system, etc.

It will also be possible to specify how **shared resources and physical devices** will be used by software tasks.

Providing the execution platform offers multiple options to allocate the tasks, the engineer will be able to interact with the tool in order to **adequately map tasks into the available resources**, depending on its criticality level and the access to shared resources and physical devices.

System Analysis

Hardware Platform Application Modelling System Analysis Code Generation	
Select analysis: FPS • Analyze	
Feasibility Table Simulation	

The engineer will be able to **model application software organized as different subsystems**. In this way, following the **abstraction and segmentation simplifying strategies** to ease the work of the engineer, each subsystem can be decomposed in a set of tasks with dependencies among them, as well as real-time properties and constraints: worst case execution time, periods, deadlines, etc.

Code Generation

The engineer will be able to **export** the analysis **results in different formats**: reports, AADL specifications, etc.

The tool will allow the engineer to **generate the proper configuration files** required by the execution platform: partition tables, task priorities, etc.

The tool will allow the engineer to automatically **generate low level code** to support the translation of analysis results: task skeletons, static plan enforcement code, etc. This code will be strongly dependent on the execution platform.

Hardware Platform	Application Modelling System Analysis <u>Code Generation</u>	
Select format: CSV	• Generate	

Flow	WCET	Deadline	Period	Response	Feasible
Flow_C	5	20	20	5	✓
Flow_B	10	40	40	15	✓
Flow_A	40	80	80	80	•

The engineer will be able to **specify the kind of system analysis** she wants to perform. She will also **interact with the tool to fix any issues** that makes the system unfeasible.

It must be **fast enough to execute "on the fly" space exploration algorithms** with some heuristics, so that the user can easily test several possible options and see the result immediately.

Hardware Platform Applica	tion Modelling System Analysis Code Generation
Select analysis: FPS - Anal	yze
Feasibility Table Simulation	
	Execution Plan
Flow_A_Task_A Flow_B_Task_B Flow_C_Task_C	0 8 16 24 32 40 48 56 64 72 80

Conclusion

Flow_C_Task_C,0,5	
Flow_B_Task_B, 5, 10	
Flow_A_Task_A, 15, 5	
Flow_C_Task_C, 20, 5	
Flow_A_Task_A, 25, 15	
Flow_C_Task_C,40,5	
Flow_B_Task_B, 45, 10	
Flow_A_Task_A, 55, 5	
Flow_C_Task_C,60,5	
Flow_A_Task_A,65,15	

elect format:	ARINC653 • Generate	
	<pre>processor implementation module.impl subcomponents Flow_A_Task_A : virtual processor partition.one; Flow_B_Task_B : virtual processor partition.two; Flow_C_Task_C : virtual processor partition.three; properties ARINC653::Module_Major_Frame => 80 ms; ARINC653::Partition_Slots => (5 ms, 10 ms, 5 ms, 15 ms, 5 ms, 10 ms, 5 ms, 15 ms); ARINC653::Slots_Allocation => (</pre>	
	reference (Flow_C_Task_C), reference (Flow_B_Task_B), reference (Flow_A_Task_A), reference (Flow_C_Task_C), reference (Flow_A_Task_A), reference (Flow end module.impl;	

A tool suite named "art2kitekt" **is being developed** as an integrated software tool for designing and analyzing mixed criticality, real-time systems. This tool chain will be capable to perform the off-line analysis, configuration and code generation for a given execution platform, while assisting the system engineer in the modeling process.

The aim **is not** to develop **another analysis tool, but a supporting tool for the analysis and design process**. The tool must guide and provide hints about how to make and tune the system. This idea is in line with a core idea of V model: test and validate your design as soon as youstart designing.

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