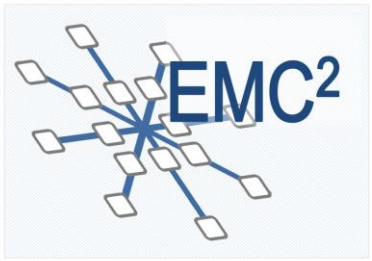

Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments

Project Acronym:

EMC²

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Publishable Executive Summary

The rapidly increasing computing power in many applications and the further trend of integration of many system functions leads to new and demanding challenges for micro-controller development of various application fields (e.g. for automotive or industrial subsystems). These subsystems (e.g. motor management of vehicles) combine sensor and actuator functions with high compute power and programmability.

Increasing computing power goes hand in hand with an increasing requirement set for accompanying power supply, measurement and support functions for the future multi-core architectures.

Furthermore, the complexity of new integrated microcontroller systems with embedded multiple cores requires new concepts of integrated power supply management architectures, new demanding concepts for measurement functions (e.g. ADCs,..) and other support functions (e.g. PLL, high speed inter-faces,…).

Based on this, the document summarizes the challenges on future power supply management architectures for integrated multi-core systems and collects the requirements for a feasibility study providing solutions for the challenges listed up in this document.

Overview of major challenges:

1. Increasing Power demand due to increasing compute performance of the compute clusters
2. Increasing Power demand due to further integration of system functionalities on a device e.g. System in Package Solutions (SiP), System on-chip Solutions (SoS)
3. Limitation in packaging and mounting space of ICs in application subsystems
4. Increased temperature range and lifetime requirements for ICs and subsystems
5. Multiple power supply rails due to big variety of interface definitions and functional constraints
6. Increasing number of use cases and functional modes of operation (stand-by, sleep, normal, etc.)
7. New Safety functions and features to ensure fail/safe operation
8. Higher robustness against external disturbance (EMC, ESD, Pulses)
9. Less interference to highly accurate measurement functions in the subsystems
10. Cope with dramatically increased leakage current in modern CMOS technologies
11. Discover new requirements and challenges raised by mixed criticality systems

The AMPS and Power Management Requirements Report derives the requirements to address solutions for new conceptual ideas and new power supply architectures to cope with these challenges of future multi core systems.

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1. Introduction

1.1 Objective and scope

The objective of the AMPS and Power Management Requirements Report is to discuss the challenges and define requirements for further feasibility studies and development of Power Management architectures and concepts to support integrated multi-core systems.

The purpose of most power management circuits, regulators or converters, is to "power" certain loads (doesn't have to be circuits) and to "manage" the energy consumed smartly, especially in the context of green electronics. In a way, power management is the design of more perfect power supply system.

In the project, it is a target to analyze how the increasing power consumption due to the higher complexity of the multi-core systems can be reduced further. One point is to find methods to increase efficiency in the complete system.

Different control mechanisms to achieve a "smart" regulator have to be discussed with the target to find the best match to cope with the challenges mentioned before. It is clear that the optimum to cover all challenges cannot be found due to different priorities depending on the application use cases, especially in the scope of mixed criticality applications.

Furthermore ideas to cope with the increasing leakage currents of highly integrated multi-core systems have to be found and suitable concepts and architecture have to be defined to prevent further increase of leakage currents

1.2 General assessment and high level requirements

A general power supply can be modeled by the block diagram in Fig. 1.1

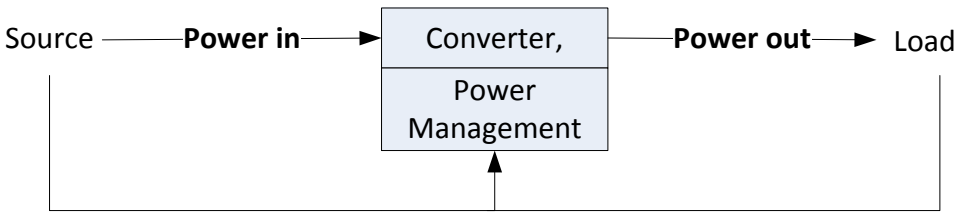

Fig. 1.1 Block Diagram for general power supply

To fulfill the power demand of a multicore system, a source of power is needed from which power can be extracted and processed. This source of power is not in the focus of our investigation hence it comes from an external power supply source (for example a battery).

In addition, a smart power supply would also use the information from both the source and the load to adjust the power conversion accordingly, often for the sake of better performance and higher efficiency.

What constitutes a good power supply?

For most electronic circuits and systems a clean, stable, and accurate supply voltage is desired for a smooth operation. Thus, most power supplies are designed to meet some or all of the following requirements:

- **Conversion:** The source and the load may not have the same form of power. The power supply needs to convert input voltage to match the need of the output.
  Four broad conversion categories can be identified: *ac-to-ac, ac-to-dc, dc-to-ac, and dc-to-dc*, and a power supply can involve one or multiple conversions.

- **Regulation:** The output voltage must be held constant within a specific tolerance for changes within a specified range in the power source and load.

- **Isolation:** The power source and load may be required to be electrically isolated completely, or partially within certain bandwidth, such that DC loading, high frequency noise, or other undesirable factors do not couple from the energy source to the load or vice versa.

- **Efficiency:** Ideally, all the power drained from the input should be delivered to the output. The power supply itself should dissipate as little energy as possible during the process.

In addition to these requirements, other factors such as size and heat dissipation may also be important.

Given these requirements, what would be a good power supply look like?

An ideal voltage source will be a perfect candidate. It provides perfect load regulation. No matter how the load impedance changes, the load voltage would always be stable. The output voltage would also be independent from its energy source, therefore bearing no influence from the input voltage.

Obviously, an ideal voltage source cannot be built in reality. It can only be approximated. Though the output voltage is meant to be independent of the input, it means a weak function of the input: V_{out}=f(V_{in}). As a result, noise and disturbance on the input source may pass through the power supply and corrupt the output signal.

Meanwhile, there exists finite output impedance R_s for the power supply. In some cases, it may even be a function of frequency and many other factors. Because of R_s, when load condition changes (e.g. reducing the resistive load), the output voltage shifts (e.g. undershoots). However, the closer the regulator (voltage controlled voltage source) resembles an ideal voltage source, the better power supply it will be.

1.3 State of the art of on chip power supply is mostly based on linear regulators

With all the advantages in their simplicity and quality, linear regulators suffer from a significant drawback: **efficiency**. The efficiency of a linear voltage regulator is defined by its output-input voltage ratio, V_{out}/V_{in}. For example, if one half of the input voltage is needed at the output, the efficiency of a linear voltage power supply would never exceed 50%, regardless of how the circuit is designed. This efficiency is due to the usage of voltage division. The pass element and the load forms a linear voltage divider (Fig. 1.2) in which the pass element always caries the total load current with $V_{DO} = V_{in} - V_{out}$ across.

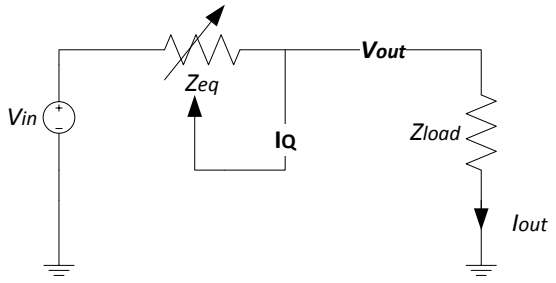

Fig. 1.2 Block Diagram of Linear Voltage Regulator

1.4 Switch mode power supply is a potential alternative to cope with the power consumption

Switch-mode DC-DC converters on the other hand do not rely on voltage division to generate the desired output. Capacitors (C) and inductors (L) are inserted into the power path as energy storage elements. Regular switching of semiconductor switches periodically reconfigures the power path, such that power is first harvested onto energy storage elements before it is delivered to the output. Since ideal L, C and ideal switches will not dissipate any power, the efficiency can reach 100% in theory.

In real application the efficiency can reach up to 90% (e.g. considering switching losses).

1.5 Further improvements with help of an intelligent Power management concept

Combining Sub-elements like Linear Regulators and Switch mode DC-DC converters together with an intelligent state machine or a Micro-Controller makes the whole architecture even more powerful and offers a higher flexibility in offering different supply concepts and different modes of operation within multi-core architectures.

1.6 Additional functionality to cope with technology impact on overall Power consumption

Due to the increasing leakage current of modern CMOS technologies the need of further conceptual ideas to reduce the power consumption in an intelligent way is absolutely necessary. Architectures and concepts have to take this into account by going new ways of active leakage reduction.

2. Requirements for Power Supply Architectures of Multi-Core Systems

2.1 Technical Requirements

1) Variable Input voltage range (e.g. 2,5V…….5,5V functional)

2) Multiple Input Supply concepts offered – examples see below
    a. Single Source 5V supply (core supply & pad supply provided by on-chip regulators)
    b. Single Source 3.3V supply (core supply provided by on-chip regulators). Regulator for Pad I/O Supply switched off – Pad I/O is supply from external
    c. Supplies are provided externally and the respective regulators are in disabled state.

3) Start-up of µC
    a. Power Management System must support any possible start-up condition as long as maximum ratings in terms of Vin and overload condition @ Pins & ambient temperature are not violated.
        i. Parameters which impacts start-up behavior are:
            1. Vin slope,
            2. residual voltage (Vin, Vout),
            3. Temperature Range
        ii. No restriction in start-up sequencing

4) Power Supply Levels and Voltage Monitoring
    a. Output voltage accuracy of voltage regulators
        i. Steady state is according state of the art requirement of actual multi-core systems (e.g.: +/-2.5% accuracy)
        ii. Dynamic functionality (load-line step) in acceptable range to ensure full function of multi-core system (e.g. -4% voltage-undershoot in case of load increase, +6% voltage-overshoot in case of load decrease),
    b. Voltage monitoring accuracy to ensure safety compliant function of multi core systems e.g. (+/-2% accuracy)

5) Power Management and Low Power Modes:
   The Power Management scheme allows activation of power down modes so that the system operates with the minimum required power for the corresponding application state.
   A progressive reduction in power consumption is achieved by invoking
    a. IDLE (peripherals continue to remain active, CPU clock disabled),
    b. SLEEP (peripherals set into sleep mode, CPU idle state entered) or
    c. STANDBY modes (voltage domain with STBY RAM keeps active) respectively.

6) Efficiency of voltage regulator should be higher than >70%

7) Maximum Output current of voltage regulator should support the needs of multi core systems to ensure full functionality without performance reduction within the systems

8) Low power mode support with acceptable supply low currents to ensure effective functionality in IDLE, SLEEP and Stand-By Modes of the multi-core system

9) Functions to reduce the Static leakage current (e.g. 20%)

10) 20 - 40 % Reduced quiescent current of multi-core system in STANDBY mode based on figures of state of the art solutions of multi core systems

11) DPI & EMC robustness according automotive requirements (e.g. BISS)

12) Support of state of the art Test concept be reducing test effort compared to actual systems
    a. e.g. BIST concepts

3. Appendix: Abbreviations

Table 1: Abbreviations

Abbreviation	Meaning
EMC^2	Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments
µC	Micro-Controller
DPI	Design and Physical Implementation
BISS	Breakthrough in Small-Signal
BIST	Built-In Self Test
AMPS	Analog-Mixed-Signal Power System