

**Embedded multi-core systems for  
mixed criticality applications  
in dynamic and changeable real-time environments**

Project Acronym:

**EMC<sup>2</sup>**

**Grant agreement no: 621429**

|                                  |  |  |
|----------------------------------|--|--|
| <b>Deliverable no. and title</b> | <b>D4.2 – Specification of Demonstrator Platforms</b>  |  |
| <b>Work package</b>              | 4  | SP Multicore Hardware Architectures and Concepts |
| <b>Task / Use Case</b>           | T4.1   | Requirements and Specifications                  |
| <b>Subtasks involved</b>         | ST4.1.1, ST4.1.2, ST4.1.3, ST 4.1.4, ST4.1.5, ST4.1.6  |  |
| <b>Lead contractor</b>           | Infineon Technologies AG<br>Dr. Werner Weber, mailto: <a href="mailto:werner.weber@infineon.com">werner.weber@infineon.com</a> |  |
| <b>Deliverable responsible</b>   | TTTech Computertechnik AG<br>Dr. Andreas ECKEL, <a href="mailto:andreas.eckel@tttech.com">andreas.eckel@tttech.com</a>         |  |
| <b>Version number</b>            | v1.0   |  |
| <b>Date</b>                      | 2014-12-19   |  |
| <b>Status</b>                    | Release Version  |  |
| <b>Dissemination level</b>       | Restricted (PU)  |  |

**Copyright: EMC2 Project Consortium, 2014**

## Authors

| <b>Partici-<br/>pant no.</b> | <b>Part.<br/>short<br/>name</b> | <b>Author name</b>           | <b>Chapter(s)</b>  |
|------------------------------|---------------------------------|------------------------------|--|
| 02D                          | TTT                             | Andreas Eckel                | Initial deliverable template and structure   |
| 04D                          | UTIA                            | Jiri Kadlec,<br>Zdenek Pohl  | Asymmetric Multiprocessing on ZYNQ   |
| 02A                          | AVL                             | Peter Priller                | Communication and verification of mixed-criticality MC control units                           |
| 18D                          | Sundance                        | Flemming Christensen         | Qt GUI Interface to control FPGAs via Ethernet, either using an Embedded CPU or a SoftCore CPU |
| 01W                          | TUDO                            | Sascha Uhrig, Lillian Tadros | SoCRocket. Time-predictable, TLM Simulation Framework  |
| 01V                          | TUBS                            | Rolf Meyer                   | SoCRocket. Time-predictable, TLM Simulation Framework  |
| 15O                          | Sevensols                       | Javier Díaz                  | Demonstrator “Dependable and high accuracy time transfer for distributed control applications” |

## Document History

| Version | Date       | Author name                              | Reason   |
|---------|------------|--|--|
| v0.1    | 27/04/2014 | Alfred Hoess                             | Initial Template   |
| v0.1    | 2014-11-14 | Andreas Eckel                            | Template for the Specification   |
| v0.5    | 11/12/2014 | Zdenek Pohl, Jiri Kadlec                 | Asymmetric Multiprocessing on ZYNQ section   |
| v0.7    | 15/12/2014 | Peter Priller                            | Communication and verification of mixed-criticality MC control units                           |
| v0.8    | 16/12/2014 | Flemming Christensen                     | Qt GUI Interface to control FPGAs via Ethernet, either using an Embedded CPU or a SoftCore CPU |
| v0.9    | 18/12/2014 | Rolf Meyer, Lillian Tadros, Sascha Uhrig | SoCRocket. Time-predictable, TLM Simulation Framework  |
| v1.0    | 18/12/2014 | Javier Díaz                              | Demonstrator “Dependable and high accuracy time transfer for distributed control applications” |
|         | 19/12/2014 | Alfred Hoess                             | Final editing and formatting, submission to ARTEMIS  |

## **Publishable Executive Summary**

The WP 4 project team has carefully identifies the following platforms suitable as “demonstration Platforms” within the frame of the EMC<sup>2</sup> WP 4 obligations:

- a) Platform based on the ACROSS approach (TUW/TTT)
- b) SoCRocket – Time-Predictable Transaction-Level Modeling Framework (TUBS/TUDO)
- c) Reliable, self-healing dynamic reconfiguration peripheral demonstration platform (TECNALIA)
- d) Platform implementing asymmetric multiprocessing on Zynq-7000 All programmable SoC with EdkDSP hardware acceleration in FPGA fabric (UTIA)
- e) Platform addressing enhanced communication and verification requirements of mixed-criticality automotive multicore control units (AVL)
- f) GUI Interface to control FPGAs via Ethernet (Sundance)
- g) Avionic demonstrator platform (Selex)
- h) Dependable and high accuracy time transfer for distributed control applications (SevenS)

Technical descriptions are provided within the document for later implementation and use within the living lab work packages.

## Table of contents

|       |   |    |
|-------|---|----|
| 1.    | Introduction.....   | 7  |
| 1.1   | Objective and scope of the document .....   | 7  |
| 1.2   | Structure of the deliverable report .....   | 7  |
| 2.    | Demonstrator Platforms Specification .....  | 8  |
| 2.1   | Platform based on ACROSS approach .....   | 8  |
| 2.2   | SoCRocket – Time-Predictable Transaction-Level Modeling Framework .....               | 9  |
| 2.2.1 | Platform Features .....   | 10 |
| 2.2.2 | Debugging Introspection .....   | 10 |
| 2.2.3 | Interconnect: IDAMC NoC .....   | 11 |
| 2.2.4 | Core Architecture .....   | 11 |
| 2.2.5 | Memory Architecture: Predictable Multi-Core Cacheability .....                        | 11 |
| 2.2.6 | Virtualization Techniques .....   | 12 |
| 2.3   | Reliable, self-healing, dynamic reconfiguration manager demonstration platform .....  | 12 |
| 2.3.1 | Introduction .....  | 12 |
| 2.3.2 | Dynamic Reconfiguration Demonstrator .....  | 13 |
| 2.3.3 | Radiation Effects Mitigation Demonstrator .....                                       | 14 |
| 2.4   | Asymmetric Multiprocessing on ZYNQ.....   | 15 |
| 2.5   | Communication and verification of mixed-criticality MC control units .....            | 15 |
| 2.6   | From FlexTiles GUI Ethernet Interface to EMC2 Turnkey Solution .....                  | 17 |
| 2.6.1 | Introduction .....  | 17 |
| 2.6.2 | EU FP7 FlexTiles Video Processing Demo .....  | 17 |
| 2.6.3 | EMC <sup>2</sup> Development Platform (DP).....                                       | 18 |
| 2.7   | Avionic Demonstrator platform.....  | 20 |
| 2.8   | Dependable and high accuracy time transfer for distributed control applications ..... | 21 |
| 2.8.1 | Introduction .....  | 21 |
| 2.8.2 | EMC2 platform for time transfer.....  | 21 |
| 2.8.3 | Expected results at the end of EMC2 .....   | 22 |
| 3.    | Conclusion .....  | 24 |
| 4.    | References .....  | 25 |
| 5.    | Abbreviations .....   | 26 |

**List of figures**

Figure 1 EMC<sup>2</sup> Many-Core Architecture based on ACROSS MPSoC ..... 9

Figure 2: SoCRocketSystemC TLM Platform ..... 10

Figure 3: Memory Architecture ..... 11

Figure 4: Virtual Clusters..... 12

Figure 5: Architecture of LADAP board..... 13

Figure 6: Reconfiguration Platform Scheme..... 13

Figure 7: Diagram describing AVL demonstrator ..... 16

Figure 8: Symmetrical FPGA Platform – EU-FP7 Flextiles Project..... 17

Figure 9: EMC2 Development Platform ..... 18

Figure 10: I/O Module ..... 19

Figure 11: EMC2 DP Modules ..... 20

Figure 12: WR-ZEN board..... 22

Figure 13: HSR network illustrating the different elements presented in the network (nodes, redbox and quadbox) 22

Figure 14: WR HSR Ring Topology. It guarantees a zero-recovery time for both PTP & Frequency distribution.... 23

**List of tables**

Table 1: Abbreviations..... 26

## **1. Introduction**

### **1.1 Objective and scope of the document**

This document will specify the demonstrator platforms to be used in the frame of the WP 4 developments within the living labs as addressed in the Technical Annex.

### **1.2 Structure of the deliverable report**

The document provides a short overview about the contents and lists the platforms considered. Within the following paragraphs the platforms are described in more detail.

## 2. Demonstrator Platforms Specification

This document will introduce the platforms for demonstration intended to be established in the frame of the EMC<sup>2</sup> project in particular concerning work conducted in Work Package 4.

The following approaches are considered:

- a) Platform based on the ACROSS approach (TUW/TTT)
- b) SoCRocket – Time-Predictable Transaction-Level Modeling Framework (TUBS/TUDO)
- c) Reliable, self-healing dynamic reconfiguration peripheral demonstration platform (TECNALIA)
- d) Platform implementing asymmetric multiprocessing on Zynq-7000 All programmable SoC with EdkDSP hardware acceleration in FPGA fabric (UTIA)
- e) Platform addressing enhanced communication and verification requirements of mixed-criticality automotive multicore control units (AVL)
- f) GUI Interface to control FPGAs via Ethernet (Sundance)
- g) Avionic demonstrator platform (Selex)
- h) Dependable and high accuracy time transfer for distributed control applications (SevenS)

### 2.1 Platform based on ACROSS approach

In the EMC<sup>2</sup> project a new many-core architecture, established on the architecture developed in the project ACROSS [1], shall be proposed. The final analysis of the ACROSS prototype identified that overall performance as a potential weakness. The cause behind this assumption is use of soft-coded processors with a limited clock rate.

In the ACROSS project five industrial demonstrators were implemented using the ACROSS architecture prototype. Although, all five demonstrators showed great success, the full performance of the architecture hasn't been fully explored. The embedded systems are becoming more complicated as the number of functions they perform increases each year. According to an embedded systems market survey in 2013 an average clock-rate of an embedded processor was 485 MHz. Also, it reports a prospect of a monotonic growth in this field over the next few years [2]. The ACROSS platform used a time-triggered network-on-chip (TTNoC), a novel on-chip communication technology with properties such as full temporal and spatial isolation, fault-tolerance, or composability. The limited performance of soft-coded processors reduces testing capabilities of the TTNoC itself. To show the full potential of the TTNoCMPSoC computing components equipped with more powerful CPUs are required.

The EMC<sup>2</sup> TTNoC architecture shall combine flexibility of an FPGA with the performance of a hard-coded processor. Besides, the components with soft-coded processors (e.g., Nios2), the EMC<sup>2</sup> TTNoC architecture shall integrate a hard processor system (HPS). The HPS is a multi-core processor system, with two ARM Cortex A9 cores [3]. In comparison with the soft-coded processors (200 MHz on average) the ARM cores run with much higher clock rate, and they should provide a significantly better performance. This way the performance limits of the architecture and the TTNoC as the on-chip communication backbone can be tested on a higher scale.

The new architecture shall include hardware modules designed in ACROSS, in particular the TTNoC of an arbitrary size, a corresponding number of trusted interface subsystems (TISSs), and system components (e.g., trusted resource manager, IO, mass-storage). Also, an HPS-TISS interconnect shall be developed, which establishes communication between an adapted TISS and the HPS. An optimal configuration for the TTNoC shall be determined based on the capacity of the FPGA and the requirements for the performance evaluation. In the Figure 1 basic building blocks of the proposed architecture are depicted.

The EMC<sup>2</sup> TTNoC architecture shall support original core services, which cover following aspects: time, communication, configuration, execution control, and diagnostics. These services are supported in

hardware and they shall be transferred to the new architecture either in full extent or in a limited form, depending on the needs of demonstrators [4].

The ACROSS architecture used the Altera Stratix IV FPGA, and for the sake of compatibility first proof of concept shall stay on an Altera platform. The EMC<sup>2</sup> TTNoC architecture shall be developed on the Altera Arria V platform. The architecture can be ported to platform like Xilinx Zynq 70xx [5], or any of the new generation Altera platforms [6].

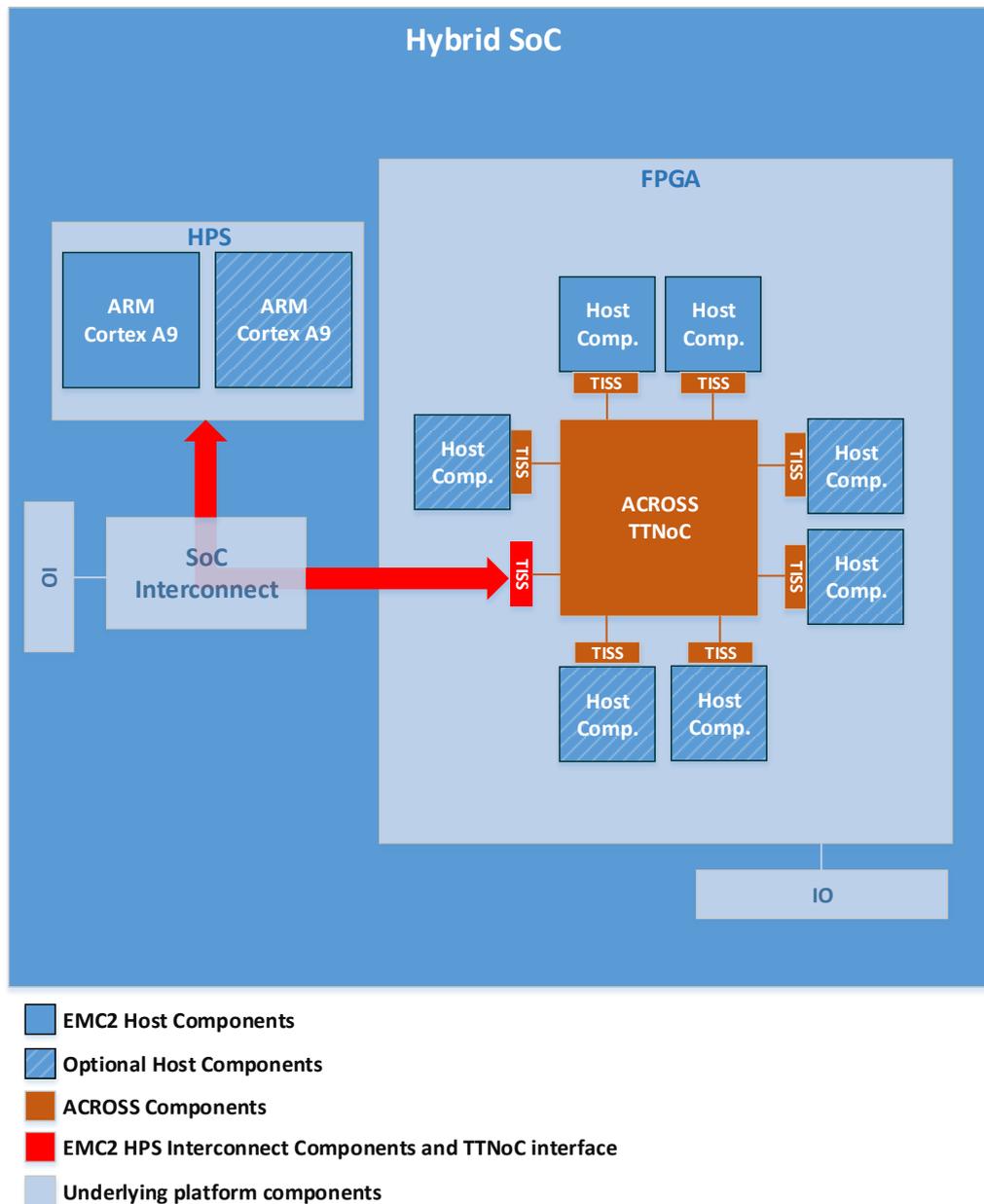


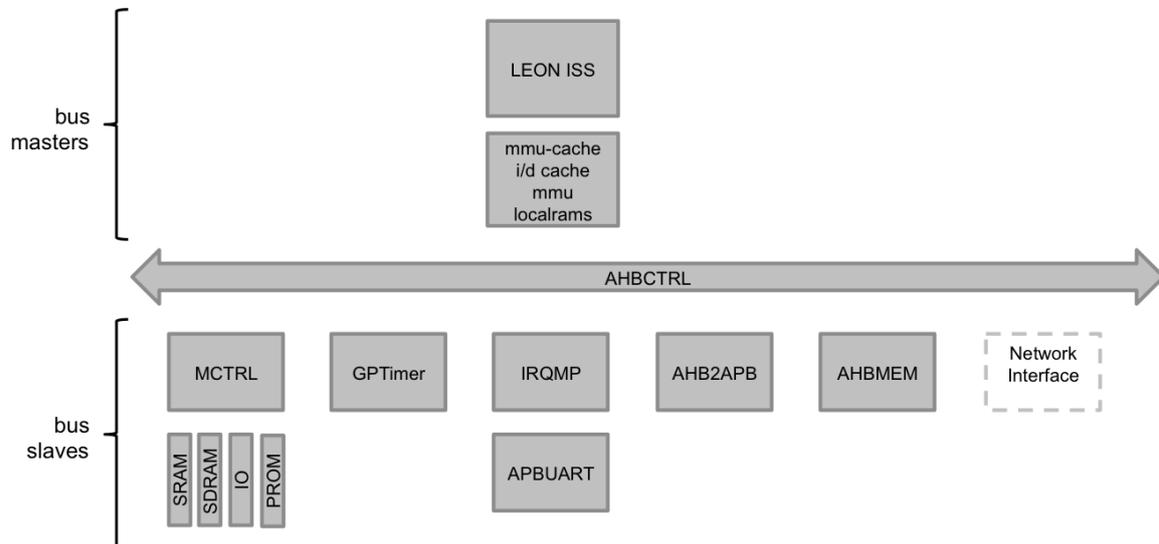
Figure 1 EMC<sup>2</sup> Many-Core Architecture based on ACROSS MPSoC

## 2.2 SoCRocket – Time-Predictable Transaction-Level Modeling Framework

Within the scope of EMC<sup>2</sup>, we will merge and expand concepts developed in the FP7 MERASA / parMERASA project with the SoCRocketSystemC / TLM platform to combine separation-of-criticalities with time-predictability in an accurate simulation platform.

### 2.2.1 Platform Features

Increasingly large portions of electronic systems are being implemented in software and its development costs start dominating the overall system's cost. Furthermore software is becoming a critical part of the development schedule, since deployment and testing on real target hardware prototypes is complicated, time-consuming and expensive.



**Figure 2: SoCRocketSystemC TLM Platform**

Transaction Level Models (TLMs) can be used to describe both timing and functionality of system components and their communication interfaces at a high abstraction level. Embedded in a virtual platform, these models are sufficiently accurate to not only allow early software development and verification in a realistic environment, but also functional verification of the modeled hardware. The capability of early design-space exploration is therefore a vital building block of full hardware/software co-design.

To achieve these goals, we designed the SoCRocket Framework. Written in SystemC/TLM, it originally fits the space industry's special needs and builds the foundation for space-domain ESL design. To enable the construction of virtual platforms, we tied together the following features:

- **Models** - All models are designed to simulate their corresponding counterparts from the [AeroflexGaislerGRLib](#)
- **Automation Tools** - To run big batches of design-space explorations
- **Infrastructure** - Reusable components for building new components at ease
- **Build System** - Extended build system for compiling models, platforms, target software.

### 2.2.2 Debugging Introspection

The debugging of such systems as mentioned before can be very time consuming and difficult due to insufficient insights into the hardware of the systems and the lack of full synchronized stops of all cores in a system. To help the software developer and hardware designer the debugging capabilities of the SoCRocket platform will be extended by better automated introspection support and direct debugger interfaces. Thus our platform can help to simplify the debugging process and will set the focus of the developer on finding the faults.

### 2.2.3 Interconnect: IDAMC NoC

The computer platforms of the future will need more processing power. This leads to a rising number of cores in embedded systems. To lower the communication synchronization overhead new models of interconnection need to be used. Our concept of raising the number of cores is to use a Network-on-Chip (NoC) to connect processing units and peripherals. Such a NoC for mixed criticality multi-core applications is the research prototype IDAMC. It has support for fault tolerance, power and performance management under real-time constraints, as well as dynamic task and interrupt re-routing in the case of faulty processing components.

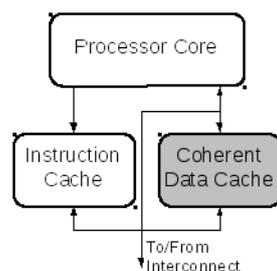
NoC-based systems consist of a high amount of complex IP building blocks. Simulating those systems at RT level takes a large quantity of time. A common strategy to reduce simulation time is removing unimportant information from the simulation. This leads to a high system abstraction model. But even simulating on a high abstraction level is a challenging task, since current simulators rarely utilize the capabilities of modern multi-core workstations. To alleviate explorations a more abstract but exact model needs to be created. For such a task a virtual platform like SoCRocket is the perfect match. With SoCRocket the focus is set on simulating multi-core systems on a high abstraction level. The results will lead to a SystemC-based model of a Network on Chip (NoC) including the cores contained in the network nodes achieving sufficient compatibility to the IDAMC approach of TUBS IDA that was previously developed. But due to the higher abstraction level easier modification and testing of new arbitration methods, quality of service functionality or other mechanisms can be accomplished in a faster way.

### 2.2.4 Core Architecture

In order to spread the platform to multiple additional domains, we will extend the platform and integrate different types of cores (e.g. ARM). This will allow homogeneous systems in FPGA (especially the wide-spread Zynq platform) and SystemC simulation. Hence, extensive design space explorations by simulations as well as hardware prototypes with a similar or even the same architecture will be possible in EMC<sup>2</sup>.

### 2.2.5 Memory Architecture: Predictable Multi-Core Cacheability

Future embedded applications will need to exploit massive fine-grained parallelism in order to deliver the required system performance. Fine-grained parallel applications can be efficient only if low-overhead communication and synchronization techniques exist, like for example shared memory. Since in multi-core architectures with higher numbers of cores or even many-cores with hundreds of cores the memory latencies increase dramatically (at least in the worst case) cache memories are required to improve memory performance. Best performance results can be reached if the caches are private to the cores. This raises the problem of cache coherence. Conventional cache coherence techniques based on the MESI or MOESI protocols lack timing analyzability and hence cannot be used in hard real-time systems. Reasons are unpredictable update or invalidation messages that are traversing the interconnections as well as unpredictable invalidations of cache lines within a local cache by remote cores.



**Figure 3: Memory Architecture**

A time predictable coherence technique has been developed in the parMERASA FP7 project. This technique will be adapted to EMC<sup>2</sup> requirements and integrated into the SoCRocketSystemC simulator. It will be compatible with bus-based systems as well as the IDAMC NoC together with multiple cores like LEON and ARM cores. If possible, it will also be integrated into FPGA prototypes, depending on the demonstrator requirements.

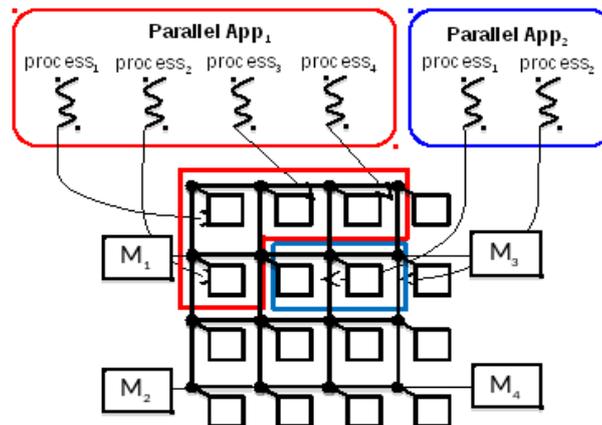


Figure 4: Virtual Clusters

## 2.2.6 Virtualization Techniques

Mixed-criticality will be addressed by core clustering and virtualization techniques. Intra- and inter-cluster synchronization will be examined to both minimize concurrency over shared resources and guarantee time-predictability. Virtualization may possibly be extended to accelerators, interconnects and the interrupt system.

## 2.3 Reliable, self-healing, dynamic reconfiguration manager demonstration platform

### 2.3.1 Introduction

In the scope of EMC<sup>2</sup> project, a peripheral to add dynamic partial reconfiguration (PR) capabilities to the LADAP platform (pictured in Figure 5) employed in the space use case will be developed by TECNALIA. Specifically the peripheral will implement PR inside the VIRTEX 5 FPGA of the hardware platform. Additionally, In order to comply with the space domain strict requirements radiations effect mitigation techniques will be included in the design.

PR is the ability to change design modules dynamically while the remaining system continues to run without interruption. In the context of space applications, it could be stated that PR addresses three main design requirements by increasing flexibility, reducing cost and size and optimizing power consumption.

The use of PR in a FPGA requires the partition of the FPGA's area in two different sections: A dynamic area where reconfigurable modules are located, and a static one, which cannot be changed dynamically, where the designed peripheral will run. The peripheral architecture, described in deliverable D4.3, is built around a Microblaze processor and a HWICAP controller for controlling reconfiguration.

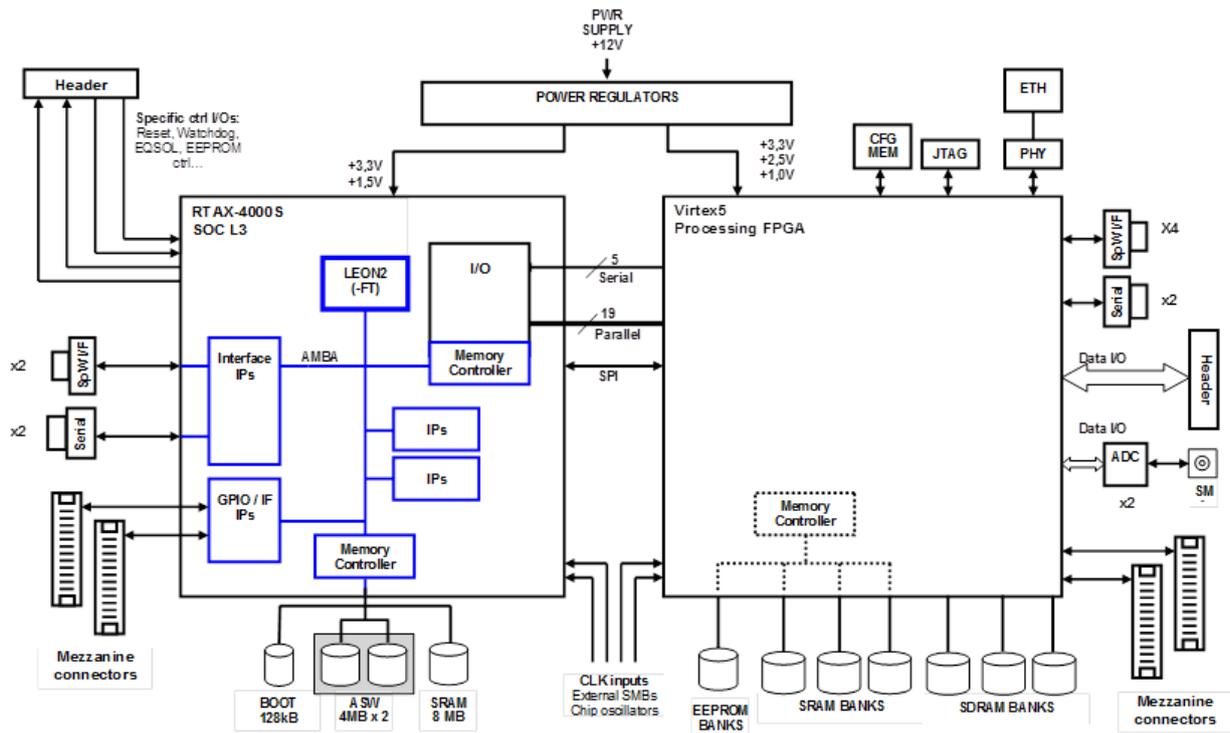


Figure 5: Architecture of LADAP board

Work in EMC<sup>2</sup> project will focus on the adaptation of the dynamic reconfiguration manager to the Space Use Case requirements by providing it with reliability and self-healing features against radiation induced effects like SEUs and SEFIs. Three mitigation techniques have been chosen for implementation.

### 2.3.2 Dynamic Reconfiguration Demonstrator

In Figure 6 a tentative scheme of the reconfiguration platform is shown. As it can be noted, the scheme is simple with a set of registers connected to the static partition embedded design to communicate with the reconfigurable modules.

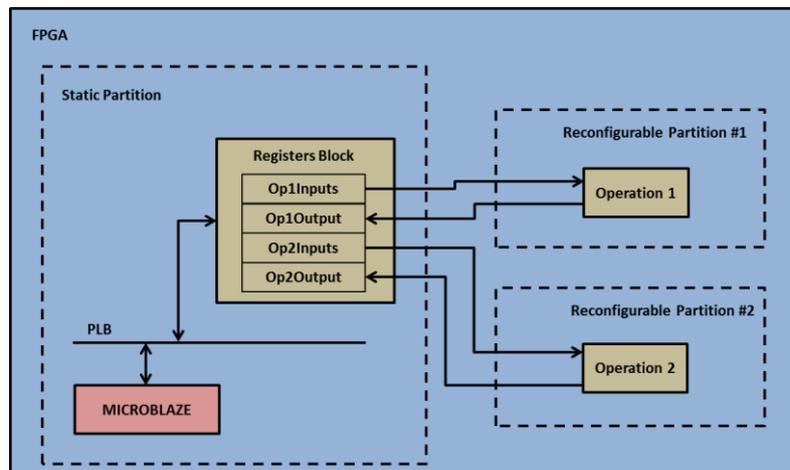


Figure 6: Reconfiguration Platform Scheme

Two different applications will be shown regarding reconfiguration:

### **Proof of Concept with simple operation**

A very simple scenario, to proof the feasibility of the system with two reconfigurable partitions that can be independently updated with one of these three designs:

- Addition operation: a module that receives two 16-bit parameters as input and provides its addition as output.
- Subtraction operation: a module that receives two 16-bit parameters as input and provides its subtraction (the higher minus the lower) as output.
- Black box: empty partition without any design.

### **Space Use Case specific application:**

This demonstration is still to be designed but it is expected to implement DSP modules such as FIR filters since they are a common operations in space applications. A DSP module will also require adding fault-tolerant design techniques to protect the non-radiation-hardened elements in the Virtex-5QV such as the DSP48E slices.

### **2.3.3 Radiation Effects Mitigation Demonstrator**

As mentioned before, most of the R&D activity within EMC2 will be focused on adding reliability and self-healing capabilities, especially to mitigate radiation induced effects. Three specific techniques are devised to detect and correct against SEUs and SEFIs.

#### **Technique 1: memory scrubbing or configuration management**

The focus of this technique is the prevention of SEU accumulation in the FPGA configuration memory. Configuration memory scrubbing will be used for re-writing the FPGA configuration memory while the design is actively running. Additionally, memory readback will be executed periodically to read configuration memory content and detect errors.

**Demonstration:** As it is impossible to do real tests with a high radiation level environment. SEUs will be emulated by software. ICAP port will be used to induce errors by programming faulty frames (frames with an incorrect CRC) in the configuration memory. Three types of error are considered to show the different performances of this mitigation technique: one-bit error, two-bit errors and more than two-bit errors.

#### **Technique 2: SEFI detection and mitigation**

SEFIs will be detected externally by a watchdog implemented in the RTAX device of LADAP platform. The designed peripheral will produce a heartbeat signal to reset this watchdog (possibly the SYNDROME\_VALID signal of the FRAME\_ECC primitive). If watchdog times out Virtex 5 FPGA must be fully reprogrammed.

**Demonstration:** As in the previous case, errors will be emulated though the mechanism is still to be defined.

#### **Technique 3: MicroBlazesoftcore protection**

MicroBlaze fault tolerance features will be enabled to protect against SEUs in the processor block RAMs. Block RAMs ECC feature can detect errors in memory contents.

**Demonstration:** Errors will be emulated by writing incorrect data in the memories.

## 2.4 Asymmetric Multiprocessing on ZYNQ

The demonstrator implements the asymmetric multiprocessing (AMP) [7] with reprogrammable, floating point, single precision, SIMD accelerator cores on Xilinx ZC702 development board [8]. It is combining:

- ARM A9 hard processor core (using  $\frac{3}{4}$  of 1GB DDR3)
- MicroBlaze FPGA processor core (using  $\frac{1}{4}$  of 1GB DDR3)
- Four EdkDSP accelerators, each with 8x SIMD floating point data paths, reprogrammable by change of firmware of the PicoBlaze6 8bit controller. Firmware can be compiled by UTIA C compiler.

The detailed architecture of the platform in its early stage can be found in deliverable D4.15 “First demonstrator platforms for use in LLs”. The platform and its later versions are provided to the EMC<sup>2</sup> through the downloadable demo package for ZC702 development kit starting by M6 of the project.

In this deliverable we will focus on the additional features to D4.15 state. The modifications take into account state and feedbacks of the EMC<sup>2</sup> partners, potential users of the platform. New features which can be supported by the platform in the EMC<sup>2</sup> include:

- **Support for FPGA fabric reconfiguration**  
The reconfiguration allows dynamically change the architecture (number of soft-core processors, number of hardware accelerators, interfaces) depending on the actual demands. It can also change the number of processors with local memories for critical applications and processors sharing the DDR with the ARM cores. The reconfiguration can happen by changing full FPGA contents or partially. It also can contribute to the increased fault tolerance since the most vulnerable part of the FPGA is the configuration SRAM. This way it can be reprogrammed in case of fault.
- **Multiplatform portability**  
The same AMP based platform can be supported for number of ZynqSoC based hardware architectures within EMC<sup>2</sup>. The possibility to implement AMP architecture for ZC702, ZedBoard, SUNDANCE Zynq module, etc. will make porting software applications between these HW platforms possible.
- **Ethernet connectivity**  
The demonstrator will implement Ethernet support by employing the FreeRTOS for non-critical applications which can include webserver, configuration bit-stream delivery, etc.

## 2.5 Communication and verification of mixed-criticality MC control units

Innovations expected from EMC<sup>2</sup> include dependable platforms for automotive control units, powered by multicore-architectures. Such setups shall allow implementation of sophisticated applications, also with differing criticality requirements, into few, powerful control units, thus reducing cost, complexity and latency. Applications foreseen include challenging goals like efficient hybrid power trains or reliable driver assistance.

While on one hand such systems provide means to reduce hardware complexity and allow efficient low latency cooperating applications, on the other hand development, verification and validation activities will become more challenging than ever. Advanced functionalities will require drastically larger number of test cases and thus parameter space to explore. Sophisticated multi-application software systems will need support for complex configuration and calibration support.

The platform developed by AVL and partners shall address such enhanced communication and verification requirements of mixed-criticality automotive multicore control units. Technologies developed

in this task will be shown in AVL’s demonstrator in WP7 / LL1, and will be applied to T7.4 “Design and validation of next generation hybrid powertrain / E-Drive”. We expect to address in particular business needs like “networking solutions for heterogeneous automotive systems” and “Tools and Methods to handle configuration of complex multicore-systems during development, calibration and diagnosis”.

Goal is to allow efficient communication in real-time between advanced test and calibration systems and the expected new generation of control units. The strong diversity of the communication protocols (both HW and SW) shall be addressed as well as challenges such as consistency, variability, authenticity of data and its structure in such a highly parallelized system within the constraints of a vehicle’s hardware.

Developments in WP4 shall investigate upcoming networking technologies like CAN-FD and automotive Ethernet for its applicability to high-performance real-time communication needed for configuration, management and verification of describe new generation control units. Time-determinisms (e.g. cyclic real-time requirements), low latency, data consistency and synchrony must be addressed in conjunction with drastically increased data throughput. Special focus shall be given to accommodate communication of multiple applications with different time and criticality requirements over a single network, as this will become a common use-case for targeted new ECU platforms. Part of this task is analysis and extension of automotive protocols like XCP for above described demands regarding support for high-bandwidth, multi-application, mixed criticality data streams.

As described, results of WP4 will be demonstrated in LL1, with a demonstrator xCU developed by ViF, based on a Aurix-Plattform (Aurix TC29xT), running FreeRTOS. This xCU will implement sophisticated algorithms for hybrid powertrain control.

Described development, debugging, testing, and calibration requirements shall be demonstrated to work over new, high-performance interfaces like CAN-FD and Automotive Ethernet technologies. The demonstrator V&V System will be based on a an x86 based multicore real-time hardware running INtime RTOS and AVL’s multicore RT Framework “AVL COBRA”. In addition to V&V, a RT Model Executer running on the same platform will provide virtual test environments as needed.

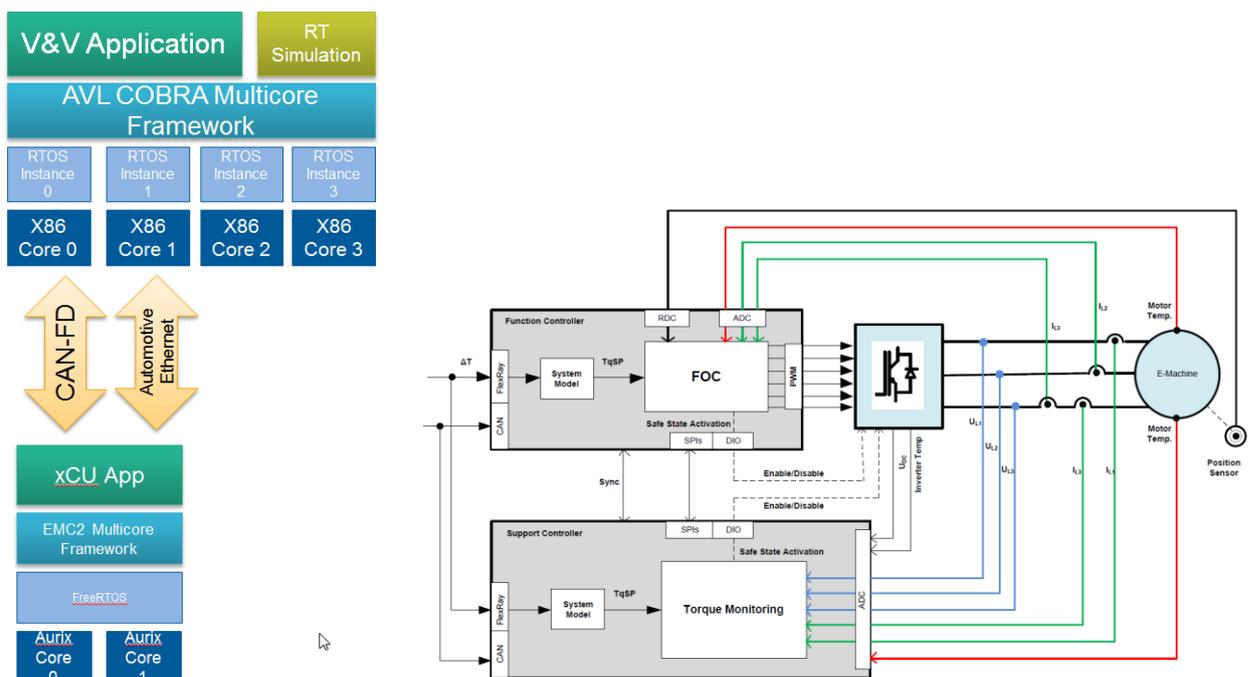


Figure 7: Diagram describing AVL demonstrator

## 2.6 From FlexTiles GUI Ethernet Interface to EMC<sup>2</sup> Turnkey Solution

### 2.6.1 Introduction

During the process of collecting “Requirements” from the EMC<sup>2</sup> Partners (Delivery D4.1) it became clear that a ‘common’ choice of a CPU from any semiconductor or CPU IP-Vendor was going to be impossible. We also established that a number of choices of the FPGA flavor was going to be required, depending on the Living Lab applications. The Space people wants the radiation proven parts, whereas the Industrial control wants the lowest power/cost. This was kind of already known during the initial proposal writing and one Sundance’s task is to: **“Engage with Leading FPGA Vendors to standardization of the EMC<sup>2</sup> Module”**

One of the few common requirements was the use the different variants of the Ethernet standard for either communication to a Host Controller, for System-to-System and even for being used as “Network-on-Chip (NoC)” between CPUs in an EMC<sup>2</sup> MultiCore fault-critical based system. It is also very easy to add any Wireless communication, being it low-speed RF in the MHz range for broad-spectrum to high-end and secure “Point-to-Point” communication in the GHz or even through fiber connections.

The only real common for all requirements is the requirement for modern, portable, flexible and widely support GUI environment to either control a EMC<sup>2</sup> system, monitor or just interface to it and this is what Sundance is aiming to do, by provide a demo the uses the Industry Standard [Qt GUI](#) that can control, monitor and interface to range of Platforms, being it Mobile or Fixed. The “Internet-of-Things” strikes again.

### 2.6.2 EU FP7 FlexTiles Video Processing Demo

Sundance, as part of the EU FP7 FlexTiles Project, developed a “Symmetrical Reconfigurable FPGA Platform”, specifically for the Partners to that is called “FlexTiles Development Platform” (FDP) and we also call it SMT166.

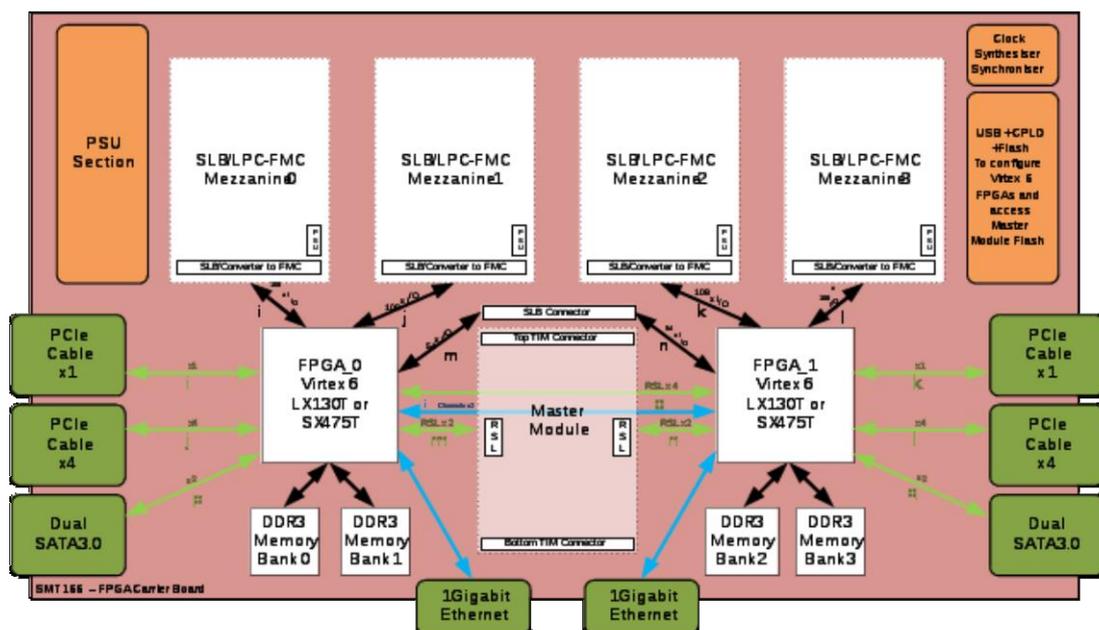


Figure 8: Symmetrical FPGA Platform – EU-FP7 Flextiles Project

The FDP has some fairly large FPGAs and also got two 1Gb Ethernet PHY and this is what we have used for the Video Processing Demo as described in D4.15 and we use a 32-bit MicroBlaze as a Host CPU. The choice of CPU is not really that important and could be replaced by an ARM SoftCore/HardCore, MIPS SoftCore, a LEON SoftCore CPU or any flavor of CPU.

The full sources for the SM166 hardware and software development that include schematics, sources are available for download (contact Sundance) and enable anybody to use Sundance's efforts for Research or even Industrial/Commercial use.

### 2.6.3 EMC<sup>2</sup> Development Platform (DP)

The "EMC<sup>2</sup>-DP", that Sundance will do as part of the WP4.6, will look like below in terms of size and format. It's a [PC/104](#) (90mm x 96mm) format and more than 1000x of compatible boards can be sourced that offers anything from low-cost CPU to Giga-bit Ethernet switches and lots of I/O options, through a infinitive Stackable PCI Express Bus with multiple lanes and lane switching (See Figure 9).

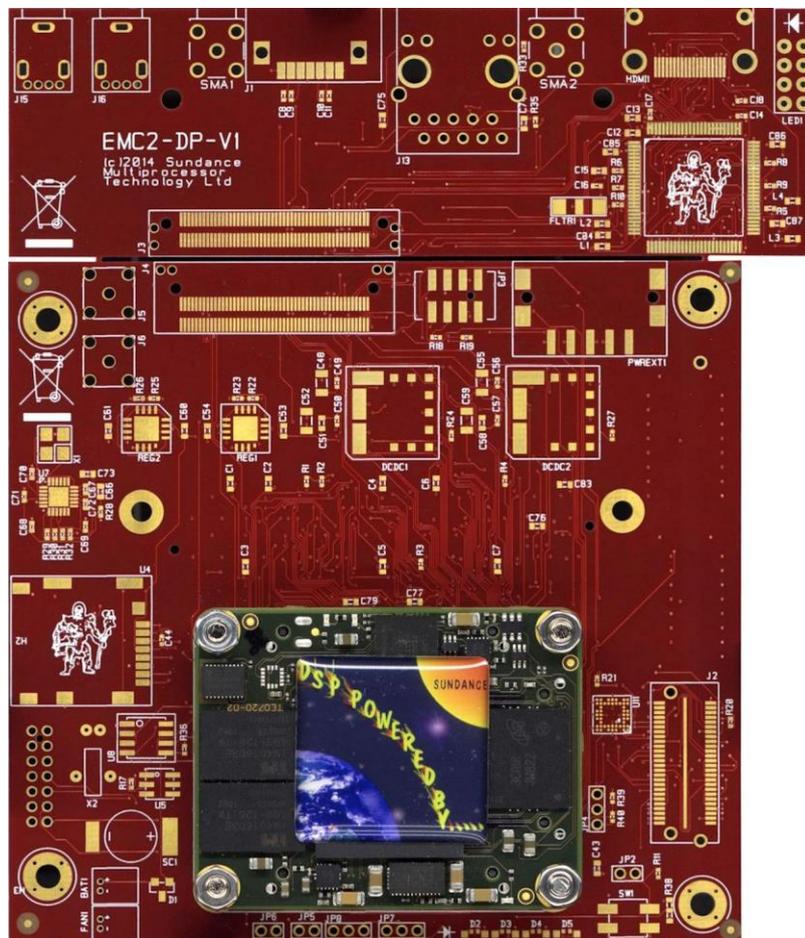
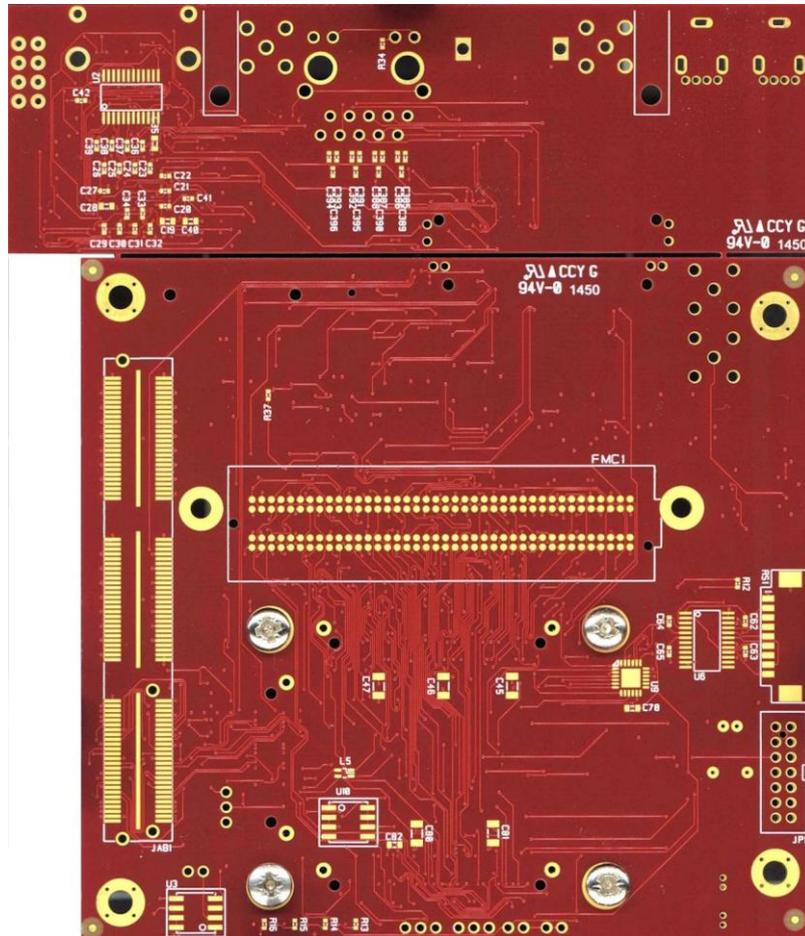


Figure 9: EMC2 Development Platform

The "EMC<sup>2</sup>-DP"'s 'Heart' is a little 50mm x 40 mm "System-on-Module", that we will for call the EMC<sup>2</sup>-SoM" and a number of variations exists now or can be developed. The current versions will be Xilinx Zynq 7015/7030, Xilinx Artix-7-100T and Kintex-7-410T, but an Intel/AMD SoC could be developed or anything else that is required, like an [Aurix](#) CPU, an [XMC1000](#) Controller and any other family of FPGA. The "EMC<sup>2</sup>-DP" has a number of on-board I/O, like SATA, HDMI, Ethernet and USB and when populated with the ARM-9 variation of the "EMC<sup>2</sup>-SoM", will run Linux.

The reverse of the “EMC<sup>2</sup>-DP” will have room for a [VITA57.1 FMC-LPC](#) I/O Module that is directly connected and controlled by the FPGA. This interface is 68x I/O pins and suitable for doing prototyping of own ‘Custom’ I/O.



**Figure 10: I/O Module**

The “EMC<sup>2</sup>-DP” will be available for the 1<sup>st</sup> review meeting of the EMC<sup>2</sup> Project with a similar Ethernet demo as Sundance has developed for the FlexTiles Platform.

Where does Sundance hope we will be in at the end of EMC<sup>2</sup> Project? The “EMC<sup>2</sup>-DP” will surely be in the hands of a number of WP4 Partners and hopefully also with some of the LL Partners and working. The initial efforts of Sundance, before the D4.1 was completed, was to design an Power-over-Ethernet Module and suitable metal enclosures to handle the max power rating of PoE, that is 24Watts. The enclosure solution will allow a “EMC<sup>2</sup>-DP” to become a total turn-key “EMC<sup>2</sup> Solution” with a PC/104 Blade system where each board is secured in a frame. This will provide a rugged enclosure and also allow expansion.



Figure 11: EMC2 DP Modules

## 2.7 Avionic Demonstrator platform

The avionics demonstrators will be based on MCP with the related main architectural/technical requirements derived from the real avionic environment. A MCP component remains however a COTS component, i.e. it features proprietary data from the COTS manufacturer: the complexity of using MCP in Mixed Critical / Hybrid avionics application, has to take into account the level of design assurance for safety reason (up to DAL A) that could increment in complexity the application (that means to including redundancy or dissimilar architecture in the architecture).

A reduction of the complexity and difficulties that arise from the use of MCPs while meeting required deterministic behavior and target levels of performance integrity has to be analyzed/detailed closely: MCP features linked to Shared Resource Accesses like Memory, Bus, Network, Internal Registers, Clock Management, etc., must be closely analyzed. These features are the differences between single-core and multicore devices, and by managing these differences the constrained multicore behavior would be made equivalent to that of multiple single-core processors.

The management can be:

- At Application Software Level: DAL-A software application to one core, lower DAL applications to other cores and programming of the arbiter to favor DAL-A software can offer determinism for this configuration;
- At Infrastructure/System level: a suitable arbiter is used to constrain the behavior of the interconnection between the core of the processor.

The target of the avionic demonstrator is to consolidate into different cores inside a multicore CPU more avionic applications (or part of that) with different DALs, which today are allocated to different processor boards. The applications will have different DAL because the functions provided by them are very different from the safety point of view.

The avionic demonstrator will implement applications related to the Flight Control System (applications with different safety levels and provide mechanisms to manage such a different safety level in a real time environment, applications that will also have different iteration rates) and a Helicopter Terrain Awareness and Warning System (HTAWS) supporting pilots in Degraded Visual Environment (DVE).

## **2.8 Dependable and high accuracy time transfer for distributed control applications**

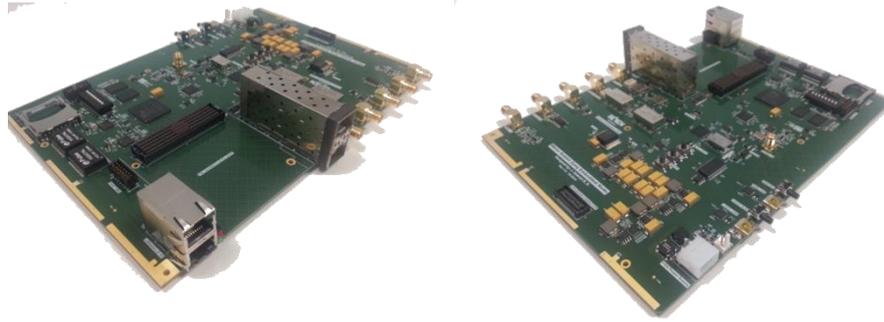
### **2.8.1 Introduction**

Our work in the framework WP4 of EMC<sup>2</sup> project is to develop mechanisms for inter-chip communication through Ethernet networks. Our main task is to implement safety-critical mechanisms for time transfer based on standard protocols like PTP (IEEE-1588) y Syn-Ethernet. We extend the concept of Quality of Service for using deterministic Ethernet-based communications for mixed-criticality systems.

Our approach is based on a modified PTPv2 protocol technology based on Ethernet optical fibers which born at CERN and it is known as White-Rabbit. This project is concerned with the industrial version of this technology supported by Seven Solutions. The robustness of the fiber optic solutions is paramount for a robust, efficient communication on industrial scenarios. The correct and reliable timing, at the nanosecond level solved by this research is of great importance for many applications and, particularly, for Smart Grid scenarios. A robust solution, highly scalable and accurate will allow extending the performance of power grids according the requirements of the next generation of applications requested by the Electricity market. The platform here developed will be used for this purpose on the WP11, user case UC5.5 Synchronized low-latency deterministic networks.

### **2.8.2 EMC2 platform for time transfer**

Our solution is based on the board called WR-ZEN. The ZEN board (Zynq Embedded Node) is a 6U stand-alone board with fully compliant FMC LPC connector mounted using a HPC footprint. It contains two optical SFP Ethernet interfaces and the FMC expansion connector allows having 2 extra GTPs, taking full advantage of high speed serial interfaces of the low cost Zynq family. On addition to FMC, an internal QSS Samtec connector is available for simple expansion boards. The board integrates the latest Xilinx Zynq Z-7015 device with a Dual ARM<sup>®</sup> Cortex<sup>™</sup>-A9 and containing an Artix FPGA-logic with 74K logic cells. It has also been designed with ultra-high stable oscillator and PLLs to provide a significant good short term stability in the order of 1 ps which makes the platform ideal not only for time transfer but also for frequency distribution.



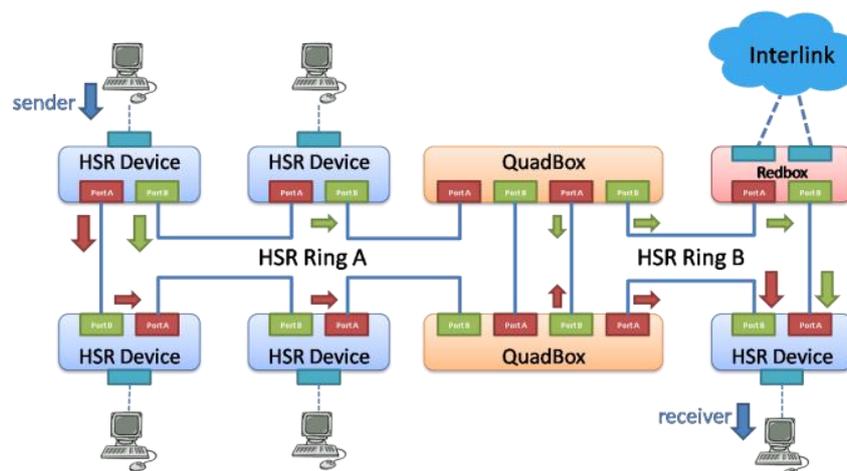
**Figure 12: WR-ZEN board**

In addition of the dual-core ARM, our gateway include a LM32 softprocessor to handle low level issues of the synchronization. It work like small Real Time processor that guarantee proper operation of low level synchronization tasks. It is programmed on stand-alone mode. Meanwhile, the user can take full advantage of the functionalities of the ARM cores for their own applications, using a customized Linux OS for non-critical application development. This approach allows having mixed-criticality system on the WR-ZEN, taking full advantage of the potential of the processors available on the Zynq device.

Currently, the target technology implements VLAN and QoS support at a beta stable. The robustness mechanism is implemented as a Rapid Spanning Tree protocol (RSTP) able to reconfigure the network whenever a node is down in the order of 30ms but still is a very preliminary stage.

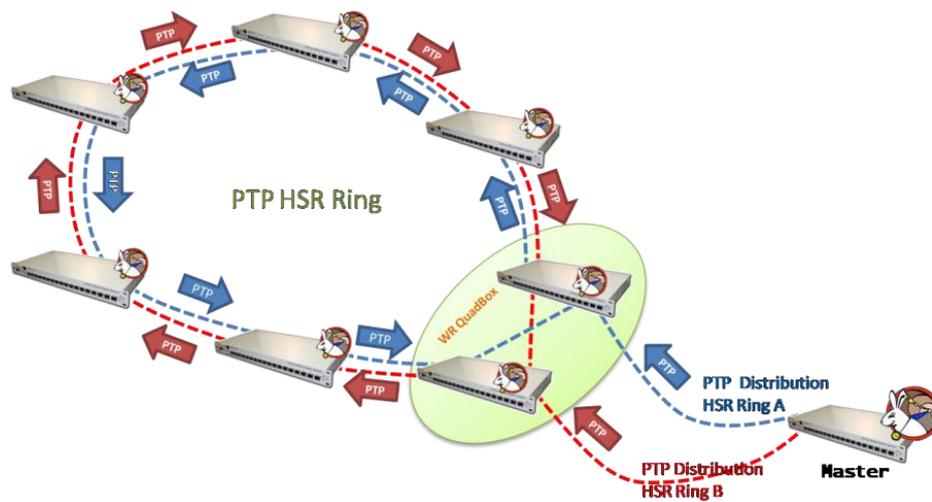
### 2.8.3 Expected results at the end of EMC2

The goal is to fully support ongoing works (VLAN and RSTP). In addition, 7S is working on the integration of a redundancy protocol to achieve zero-time recovery in networks. This protocol is known as High-availability Seamless Redundancy (HSR, IEC 62439-3) and guarantees zero-time recovery in case of failure and low latencies. Including the protocol in our White-Rabbit devices, we could extend HSR features to time and frequency distribution in high accuracy time transfer ring networks.



**Figure 13: HSR network illustrating the different elements presented in the network (nodes, redbox and quadbox)**

For this purpose, 7S is working on a HSR IP-Core that will be included in next-gen nodes to enable HSR configurations to guarantee that, in case of failure, both time and frequency will remain synchronized with no loss.



**Figure 14: WR HSR Ring Topology. It guarantees a zero-recovery time for both PTP & Frequency distribution.**

The final outcome of the project will be a demonstrator of a deterministic, highly accurate time and frequency dissemination mechanism based on the WR-ZEN board. It will illustrate the different mechanisms developed in WP4 and used on an extended demonstrator in the framework of Smart Grid applications.

### **3. Conclusion**

The described platforms, which will be developed within the frame of WP4, major advances are planned within the living lab work packages. They will be integrated in the planned approaches according to the planned activities as laid down in the EMC<sup>2</sup> technical annex.

## 4. References

- [1] C. El Salloum, M. Elshuber, O. Höftberger, H. Isakovic und A. Wasicek, „The ACROSS MPSoC - A new generation of multi-core processors designed for safety-critical embedded systems,“ *Microprocess. Microsyst.*, Bd. 37, Nr. 0141-9331, pp. 0141-9331, 2013.
- [2] U. Tech, „UBM Electronics 2013 Ebedded Market Study,“ 2013. [Online]. Available: <http://e.ubmelectronics.com/2013EmbeddedStudy/>. [Zugriff am 2014].
- [3] H. Isakovic, „Specification of High-performance TTNoC Many-Core Architecture,“ 2014.
- [4] A. Corporation, „Arria V SoC Development Kit and SoC Embedded Design Suite,“ 20 11 2014. [Online]. Available: <http://www.altera.com/products/devkits/altera/kit-arria-v-soc.html>.
- [5] X. Inc., „Zynq-7000 SiliconDevices,“ 2014. [Online]. Available: <http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/silicon-devices.html>. [Zugriff am 2014].
- [6] C. Altera, „Next generation technologies,“ 2014. [Online]. Available: <http://www.altera.com/technology/system-tech/next-gen-technologies.html>.
- [7] „XilinxMicroblaze AMP, application note,“ [Online]. Available:[http://www.xilinx.com/support/documentation/application\\_notes/xapp1093-amp-bare-metal-microblaze.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp1093-amp-bare-metal-microblaze.pdf).
- [8] „ZC702 Development board,“ [Online]. Available: [http://www.xilinx.com/support/index.html/content/xilinx/en/supportNav/boards\\_and\\_kits/zynq-7000\\_soc\\_boards\\_and\\_kits/zynq-7000\\_soc\\_zc702\\_evaluation\\_kit.html](http://www.xilinx.com/support/index.html/content/xilinx/en/supportNav/boards_and_kits/zynq-7000_soc_boards_and_kits/zynq-7000_soc_zc702_evaluation_kit.html).

## 5. Abbreviations

**Table 1: Abbreviations**

| Abbreviation | Meaning   |
|--------------|---|
| ACROSS       | ARTEMIS Cross Domain Architecture   |
| AMP          | Asymmetric Multi-Processing   |
| COTS         | Commercial Off The Shelf  |
| CRC          | Cyclic Redundancy Check   |
| DAL          | Design Assurance Level  |
| DSP          | Digital Signal Processor  |
| ECC          | Error Correcting Code   |
| EMC2         | Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments |
| FIR          | Finite Input Response   |
| FPGA         | Field-Programmable Gate Array   |
| μC           | Micro-Controller  |
| HPS          | Hard Processor System   |
| HWICAP       | Hard Ware Internet Content Adaptation Protocol  |
| HTAWS        | Helicopter Terrain Awareness and Warning System   |
| ICAP         | Internet Content Adaptation Protocol  |
| IDAMC        | Integrated dependable Architecture for Many Cores   |
| MCP          | Mode Control Panel  |
| MESI         | Modified, Exclusive, Shared, Invalid – Cache coherence protocol   |
| MOESI        | Modified, Owned, Exclusive, Shared, Invalid – Cache coherence protocol  |
| RTAX         | Radiation Hard FPGA type by Microsemi   |
| RTOS         | Real Time Operating System  |
| SEFI         | Soft Error Fault Injections   |
| SEU          | Single Event Upset  |
| SIMD         | Single Instruction, Multiple Data   |
| TISS         | Trusted Interface Sub-System  |
| TLM          | Transaction Level Modeling  |