

Asymmetric Multiprocessing on industrial ZYNQ board with HDMI I/O

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Abstract – This paper describes two system on chip designs for the industrial grade Trenz electronic TE0720-02-2I System on Module (SOM) and the TE0701-05 carrier board. The asymmetric multiprocessing designs are integrating on ZYNQ one ARM Cortex A9 processor with vector floating point accelerator NEON, one MicroBlaze processor and four run-time reprogrammable (8xSIMD) EdkDSP floating point accelerators in the programmable logic of ZYNQ. The HDMI I/O describes four different designs demonstrating the HDMI output HDMI input and Vita 2000 color video sensor input, in full HD resolution (1920x1080p60). All designs are precompiled in Xilinx Vivado 2015.2 and aim to support the Software Defined System on Chip tool chain SDSoc 2015.2 introduced in summer 2015 by Xilinx. All designs aim to be in the future portable to the EMC2-DP platform developed by Sundance. Designs have been developed in frame of the Artemis project EMC2.

Keywords – software defined system on chip; asymmetric multiprocessing; floating point; reconfigurable accelerators

I. INTRODUCTION TO HETEROGENEOUS ASYMMETRIC MULTIPROCESSING SYSTEM ON CHIP WITH FLOATING POINT EDKDSP ACCELERATORS

The asymmetric multiprocessing (AMP) design described in this paper is based on the Xilinx application note XAPP1093 [1]. The AMP design has been ported from the ISE 14.5 design flow to the Xilinx Vivado 2015.2 and SDK 2015.2 design flow.

The ARM Cortex A9 processor [4] works together with the MicroBlaze processor, sharing the terminal and block ram. Both processors execute program from the same external DDR3 memory. The MicroBlaze processor is controlling 4 EdkDSP floating-point accelerators. Each accelerator is organised as 8xSIMD reconfigurable data path, controlled by the PicoBlaze6 controller [7].

The developed industrial grade SoC and the related evaluation package is provided by UTIA for the Trenz electronic TE0720-02-2I System on Module [2] and the TE0701-05 carrier board [3]. These features are demonstrated in this paper:

- Implementation of adaptive acoustic noise cancellation on 1 of 4 accelerators is computing the recursive adaptive LMS algorithm for identification of regression filter with 2000 coefficients in single

precision floating point arithmetic with sustained performance

- 777 MFLOP/s on single 125 MHz (8xSIMD) EdkDSP accelerator
- 338 MFLOP/s on single 666 MHz ARM Cortex A9 (with the vector NEON unit)
- 160 MFLOP/s on single 666 MHz ARM Cortex A9 (with the 32bit floating point unit)
- 10 MFLOP/s on single 125 MHz MicroBlaze processor (with the 32bit floating point unit)
- The EdkDSP accelerators can be reprogrammed by firmware. The programming is possible in C with the use of the UTIA EDKDSP C compiler. Accelerators can be programmed with two firmware programs. Designs can swap in the real time the firmware in only few clock cycles in the runtime.
- The floating-point applications are scheduled inside of the 8x SIMD EdkDSP accelerator by the Xilinx PicoBlaze6 processor [7]. Each firmware program has maximal size of 4096 (18 bit wide words). The alternative firmware can be downloaded to the EdkDSP accelerators in parallel with the execution of the current firmware. This is demonstrated by swap of the firmware for the FIR filter room response to the firmware for adaptive LMS identification of the filter coefficients in the acoustic noise cancellation demo.
- The 8xSIMD EdkDSP accelerator is providing single-precision floating-point results bit-exact identical to the reference software implementation running on MicroBlaze processor with the Xilinx floating point unit.
- The 125 MHz 8xSIMD EdkDSP accelerator is 2,3x faster than the 666 MHz ARM Cortex A9 (with NEON vector processing unit) 4,8x faster than the 666 MHz ARM Cortex A9 without code optimized for NEON and 78x faster than 125 MHz MicroBlaze with HW floating point unit. These data are measured for the presented case of the 2000 tap adaptive LMS filter.
- The floating-point 2000 tap coefficients FIR filter (acoustics room model) is computed by single 125

MHz (8xSIMD) EdkDSP accelerator with the floating point performance 1234 MFLOP/s. The peak performance of the single 125 MHz (8xSIMD) EdkDSP accelerator is 2 GFLOP/s.

- The peak performance of four 125 MHz (8xSIMD) EdkDSP accelerators implemented in this demo design is 8 GFLOP/s.

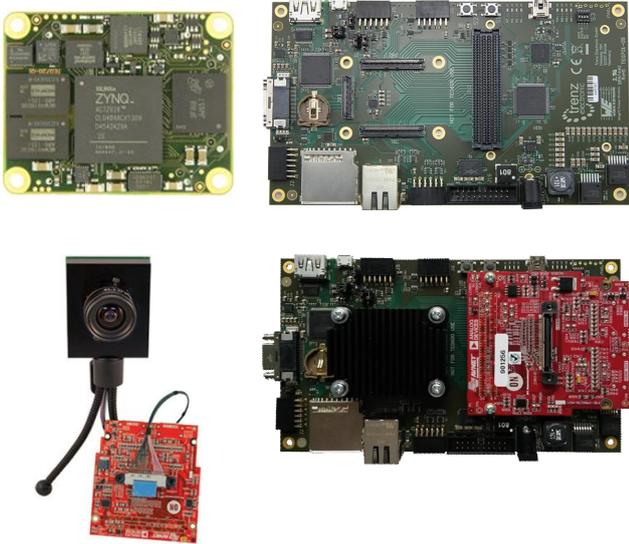


Fig. 1 Trenez electronic TE0720-02-2I System on Module (SOM), TE0701-05 carrier board and Imageon FMC board for HDMI I/O and HD video sensor.

The bce_fp12_1x8_0_axiw_v1_40 EdkDSP accelerator IP core performs:

- Vector floating point operations FPADD, FPSUB in 8 SIMD data paths.
- Vector floating point MAC operations in 8 SMD data paths for length of the vector 1 up to 10. These accelerators can be used in applications like floating point matrix multiplication with row and column dimensions ≤ 10 .
- Floating-point vector-by-vector dot products performed in 8 SIMD data paths. It is optimized for parallel computation of up to 8 FIR or LMS filters, each with size up to 255 coefficients. It is also effective in case of floating-point matrix-by-matrix multiplications, where one of the dimensions is large (in the range from 11 to 255).
- Additional HW support of dot product. It is computed in 8 data paths with the HW supported wind-up into single scalar result.
- Support for single data path the pipelined vector floating point division. Accelerators is suitable for applications like adaptive recursive (normalised) NLMS filters and the square root free versions of

adaptive RLS QRD filters and adaptive square root free RLS QRD LATTICE filters.

- The system clock of ARM Cortex A9 is 666 MHz, MicroBlaze 125 MHz and EdkDSP accelerators 125 MHz.
- The EdkDSP floating-point accelerators are reconfigurable during runtime by change of firmware.
- Asymmetric multiprocessing of ARM Cortex A9 and MicroBlaze system with shared external DDR3.

AMP EdkDSP HW evaluation designs have been compiled in Xilinx VIVADO 2015.2 [5] with SW projects for SDK 2015.2 [6]. Presented HW accelerators can results in better POWER per MFLOPS ratio for certain class of DSP applications in comparison to the computation on standard CPUs with standard HW floating point support. The AMP EdkDSP demonstrator includes source code of set of SW demos prepared for easy import of projects and compilation in the Xilinx SDK 2015.2 [6].

II. RESOURCES USED BY THE DESIGNS

Table 1 and Table 2 present resources used by both designs.

TABLE 1- AMP DESIGN ON ZYNQ, ARM A9, MICROBLAZE AND 1X (8xSIMD) EDKDSP

7z020-1	fp32	fp32	fp32	fp32	fp32
EdkDSP vector op.	Add	Mac	Dot Prod	S8 Prod	div
fp12_1x8_40	8x	8x	8x	1x	1x
7z020-1	Resources (complete PL) EdkDSP performance				
EdkDSP vector op.	FF %	Lut %	Bram no (of)	LMS Mflop/s	FIR Mflop/s
fp12_1x8_40	10	21	48 (140)	777	1234

TABLE 2 - AMP DESIGNS ON ZYNQ, ARM A9, MICROBLAZE AND 4X (8xSIMD) EDKDSP

7z020-1	fp32	fp32	fp32	fp32	fp32
EdkDSP vector op.	Add	Mac	Dot Prod	S8 Prod	div
fp12_1x8_40	8x	8x	8x	1x	1x
7z020-1	Resources (complete PL) EdkDSP performance				
EdkDSP vector op.	FF %	Lut %	Bram no (of)	LMS Mflop/s	FIR Mflop/s
fp12_1x8_40	10	21	48 (140)	777	1234

A. Asymmetric multiprocessing and use of external DDR3 memory maintaining the Integrity of the Specifications

Presented FPGA designs are running on the Trenez electronic TE0720-02-2I System on Module [2] and the TE0701-05 carrier board [3]. See Fig. 1. It is using the 1GB DDR3 memory with clock signal 533 MHz. The DDR3 is connected to Xilinx ZYNQ xc7z020-2I FPGA by 32 data path. The first $\frac{3}{4}$ of the DDR3 are reserved for the ARM A9 processor. The last $\frac{1}{4}$ is used by the MicroBlaze processor with the EdkDSP accelerators. The presented AMP demo is extending the Xilinx application note XAPP1093 [1] solution from the Xilinx ISE/EDK 14.5 flow to the Xilinx Vivado

2015.2 design flow. See Fig. 2 for the architecture of the design.

B. Re-programmability of EdkDSP accelerators

Each of the four 125 MHz 8xSIMD EdkDSP floating-point accelerator subsystems contains one reprogrammable Xilinx PicoBlaze6 8-bit processor and the floating point 8xSIMD DSP unit. The performance of the accelerator is application specific. In this demo, a single 8xSIMD EdkDSP unit is delivering sustained 1234 MFLOP/s in case of 2000 tap FIR filter computation and 777 MFLOP/s in case of the adaptive 2000 tap LMS filter identification demo. The Xilinx PicoBlaze6 [7] controller has fixed configuration with size of the program memory 4096 (18 bit wide) words, 64 Bytes scratch pad RAM memory and the interrupt vector in the address 1023. Both PicoBlaze6 program memories are accessible by the MicroBlaze processor via AXI-lite bus. The PicoBlaze6 controller can execute program from each of these memories. The MicroBlaze application can write new firmware to the currently unused program memory, while the EdkDSP accelerators and their PicoBlaze6 controllers are executing firmware from second program memory.

C. Debug of the AMP system with EdkDSP accelerators in the evaluation package

All EdkDSP accelerators can communicate with MicroBlaze program. The communication is using the UTIA Worker Abstraction Layer (WAL) library API. This API is also used for support of writing of the debug information from the worker to the MicroBlaze terminal.

memory controller of the ZYNQ processing system [4]. See Fig. 2.

ARM and MicroBlaze can be both debugged simultaneously from the SDK 2015.2 GDB debugger integrated in the Xilinx SDK tool [6]. PicoBlaze6 controllers [7] can exchange data and text via the 8 bit communication data paths and AXI-lite bus with the MicroBlaze processor. This path is used to communicate parameters to the accelerators and to get messages or reports from accelerators for debugging.

Floating-point data are accessed by the MicroBlaze processor via the dual ported block memories of accelerators. The MicroBlaze sides of the dual-portted accelerator memories are all mapped into the MicroBlaze memory space. The MicroBlaze processor can copy data from these dual ported memories to its global DDR3 workspace and display floating point data in the debugger.

The computation in the (8xSIMD) EdkDSP units can overlap with communication with the DDR3. It is performed by UTIA libwal.a API provided as MicroBlaze library and it is supported by MicroBlaze Data and program cache. A Ping-Pong swap of memory banks is used. The 8xSIMD EdkDSP firmware scheduling the parallel (8xSIMD) computation in some banks of accelerator memories.

The MicroBlaze program is communicating (sequentially) to/from DDR3 in another set of banks of the dual-portted accelerator memories. This process can be stopped, inspected and debugged by the MicroBlaze debugger from the SDK debugger [6] in the synchronization functions defined in the UTIA libwal.a API.

III. ASYMMETRIC MULTIPROCESSING DEMO

- `õamp_cpu_1x8_allõ` project in the `õProject Explorerõ` window of the SDK 2015.2 [6] is used to program ARM A9 part of the AMP demo.
- `õedkdsp_fp12_4x8_allõ` project is used to program the MicroBlaze core and the four EdkDSP accelerators of the AMP demo.
- `õedkdspõ` project contains `libwal.a` library for the MicroBlaze processor.
- `õedkdsp_ccõ` directory contains C source code for the PicoBlaze6 controller firmware and UTIA EDKDSP C compiler binary for compilations of C and ASM code [7] for the PicoBlaze6 controller of the EdkDSP accelerators.
- The UTIA EDKDSP C compiler can be executed in Win 7 64 bit under the VMware Workstation 12 Player [19] running in the preconfigured 32bit Linux Ubuntu image (provided by UTIA for free) the 32 bit the compiler binary application (provided by UTIA for free).

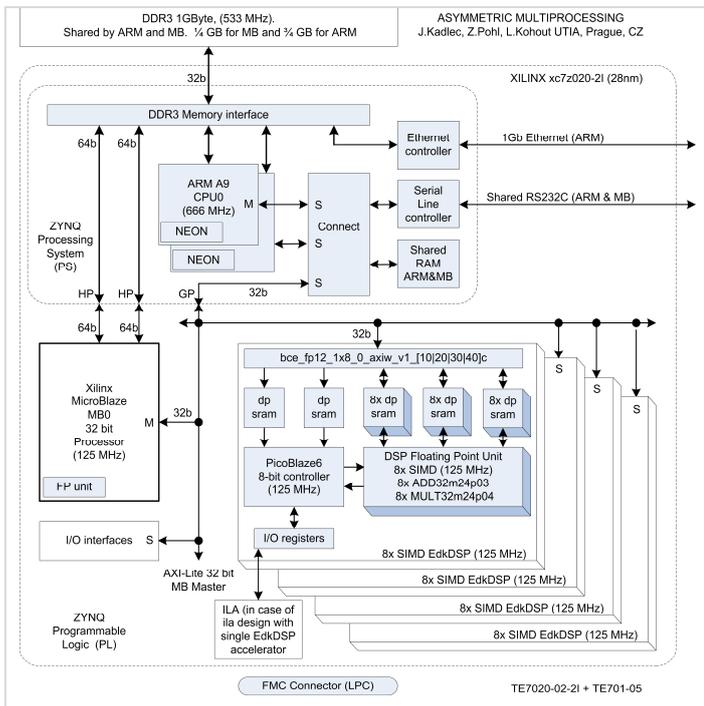


Fig. 2 Simplified architecture of AMP with four EdkDSP accelerators

MicroBlaze is using the terminal of the ARM A9 processing system, present in the ZYNQ processing system [4]. ARM A9 and MicroBlaze communicate via the internal shared

IV. PERFORMANCE OF ARM A9 NEON AND EDKDSP ACCELERATOR

The performance of processors and accelerators is dependent on the optimization level of C compiler for ARM and C compiler for MicroBlaze. Lines labeled FIR ARM. Table 3 and Table 4 document how the ARM performance improves with the Compiler optimization level. Additional substantial improvement can be reached only with manual transformation of the C source code ARM A9 processor.

TABLE 3- MEASURED PERFORMANCE IN MFLOP/S FOR FIR FILTER COMPUTATION

FIR MFLOP/s	-O0	-O1	-O2	-O3
FIR ARM (666 MHz)	36	105	120	152
FIR ARM NEON (666 MHz)	56	351	342	466
FIR MB EdkDSP (125 MHz)	1234	1234	1234	1234

TABLE 4 - MEASURED PERFORMANCE IN MFLOP/S FOR LMS FILTER COMPUTATION

LMS MFLOP/s	-O0	-O1	-O2	-O3
LMS ARM (666 MHz)	42	115	137	150
LMS ARM NEON (666 MHz)	49	284	277	352
LMS MB EdkDSP (125 MHz)	777	777	777	777
LMS MB (125 MHz)	3	7	10	10

This is visible in the lines FIR ARM NEON and LMS ARM NEON. The corresponding functions have been reorganized to group together parallel computation of 4 floating point MAC operations in parallel. This resulted in better use of the vector capabilities of the NEON unit.

The EdkDSP (8xSIMD) accelerator works with hand optimized code for the FIR and the LMS filter. The optimization levels of the MicroBlaze C compiler have impact on the MicroBlaze processor performance and only minimal influence on performance of the EdkDSP accelerators.

V. ASYMMETRIC MULTIPROCESSING DEMO WITH SINGLE EDKDSP ACCELERATOR WITH IN-CIRCUIT LOGIC ANALYSER (ILA)

The evaluation design with ARM A9 [4] processor and MicroBlaze processor with single (8xSIMD) EdkDSP can be extended by the Vivado In-Circuit Logic Analyzer (ILA). It is part of the free Vivado Lab Edition 2015.2 [21].

TABLE 5 - AMP DESIGN WITH ILA ON ZYNQ, ARM A9, MICROBLAZE AND 1X (8xSIMD) EDKDSP ACCELERATOR.

7z020-1	fp32	fp32	fp32	fp32	fp32
EdkDSP vector op.	Add	Mac	Dot	S8	div
fp12_1x8_40	Mul	8x	Prod	Prod	1x
7z020-1	Resources (complete PL) EdkDSP performance				
EdkDSP vector op.	FF %	Lut %	Bram no (of)	LMS Mflop/s	FIR Mflop/s
fp12_1x8_40	16	37	114 (140)	777	1234

The implemented precompiled In-Circuit Logic Analyzer (ILA) can store 32k samples of all output signals of the (8xSIMD) EdkDSP Accelerator labeled for the debug.

Debug ports provide visibility of the vector (8xSIMD) EdkDSP accelerator. Debug probes help to trace the integer addresses and the vector operation schedules. Floating-point data are not displayed. These data can be better analyzed in the MicroBlaze debugger [4]. MicroBlaze programs can access all dual-ported memories of the of the (8xSIMD) EdkDSP accelerator and copy these data to user-defined arrays declared in the DDR3 in the user workspace of the MicroBlaze C application for debug in SDK 2015.2 debugger [6].

D. ILA debug ports of the (8xSIMD) EdkDSP accelerator.

- bce_atoa[0:9] Memory A address (addressing 1024 32 bit floating point values).
- bce_atob[0:9] Memory B address (addressing 1024 32 bit floating point values).
- bce_atoz[0:9] Memory Z address (addressing 1024 32 bit floating point values).
- bce_done[0:7] Vector operation in progress or finished.
- bce_led4b[0:3] 4bit output, intended for led signaling. Unconnected in the design.
- bce_mode[0:3] Mode of communication protocol PicoBlaze6 - MicroBlaze.
- bce_op[0:7] Vector operation to be performed.
- bce_port[0:7] Data on external port.
- bce_port_id[0:7] External port address. Address space [0x0 ... 0x1F] are reserved for internal construction of the WLIW instruction to the 8xSIMD vector processing unit of the EdkDSP. Address space [0x20 ... 0xFF] can be used by the user.
- bce_port_wr Write strobe related to writing of 8bit data to the external port address.
- bce_r_pb Reset of the PicoBlaze6.
- bce_we Write strobe related to writing of a WLIW instruction to the 8xSIMD vector processing unit of the EdkDSP.

These signals can be all used for real-time analysis of the computation inside of the 8xSIMD vector-processing unit of the EdkDSP. This helps with the debug of the coordination of the PicoBlaze6 firmware code, the vector-processing unit together with MicroBlaze code.

The ILA triggering combination of probe signals can be initiated and modified from the EdkDSP firmware running on the PicoBlaze6 controller. This firmware can be modified SDK 2015.2 editor and recompiled by the UTIA EDKDSP C compiler running in [19].

Selected markers indicate single elementary step of the FIR filter. See Fig. 3. It takes 308 clock cycles (125 MHz = 8ns clock period) to compute the vector product of two floating-point vectors (coefficients and data), both with length $248 \times 8 = 1984$ elements and to update the data vector (circular buffer). The ILA HW support provides sufficient level of visibility and debug capabilities for the developer of the (8xSIMD) EdkDSP firmware.

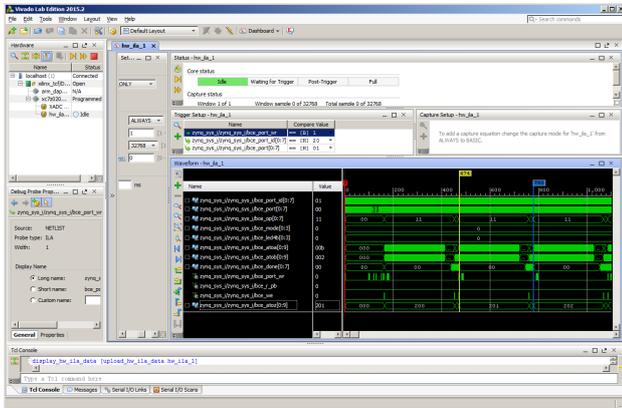


Fig. 3 Vivado Lab Edition 2015.2 ILA display of the FIR filter computation

The red trigger is corresponding to the event. We can zoom in the data and define additional markers. Selected markers to indicate single elementary step of the LMS filter. It takes 1154 clock cycles (100 MHz = 8ns clock period) to compute the vector product of two floating point vectors (coefficients and data), both with length $248 \times 8 = 1984$ elements, update the data vector (circular buffer), compute the prediction error and adapt the coefficients of the LMS filter.

The `bce_op[0:7]` debug signal is displayed in the analogue/hold mode and indicates the sequence of vector operations issued by the PicoBlaze6 firmware, while implementing the single LMS step on single (8xSIMD) EdkDSP vector unit.

The ARM code and the MicroBlaze code can be compiled with `o0, i, -O3` optimizations and executed under both debuggers in combination with ILA triggering. The `o0` option provides lower performance on ARM and MicroBlaze, but the corresponding code includes no transformations. This makes the debugging of C code easier. This helps in debugging of the interactions of AR A9, MicroBlaze and EdkDSP accelerator. Complete exchanged blocks of floating point data can be inspected and verified in the MicroBlaze GDB debugger in SDK 2015.2 [6]

The EdkDSP accelerator code is deterministic and all operations can be emulated in the MicroBlaze C code, including the exact sequence of all floating-point operations. The floating-point unit cores of the MicroBlaze for the ADD and MULT provide bit-exact identical results to the floating-point units used in the (8xSIMD) EdkDSP vector unit. This determinism secures, that the MicroBlaze code provides bit-exact identical results to the (8xSIMD) EdkDSP vector unit. This is used for verification of accelerated algorithms.

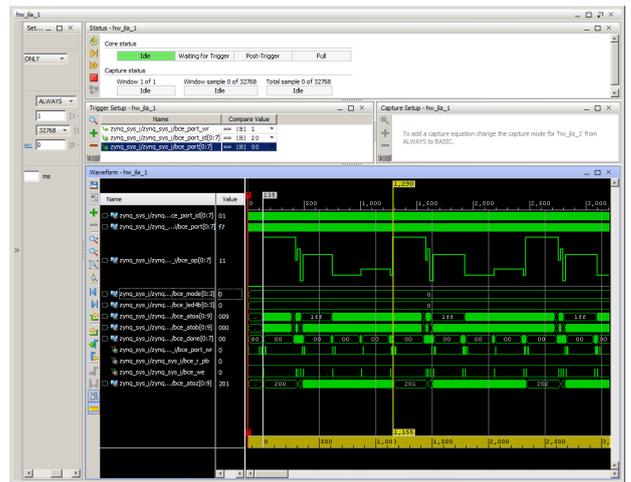


Fig. 4 Vivado Lab Edition 2015.2 ILA display of adaptive LMS filter computation

VI. CONDITIONS FOR USE, DOWNLOADS

This demonstrator is provided by partner UTIA.

- The demonstrator includes evaluation versions of AMP designs for ZYNQ. Designs work with one ARM Cortex A9 processor, one MicroBlaze processor and four instances of the EdkDSP accelerators with 8xSIMD floating point data paths. Evaluation designs are precompiled in Vivado 2015.2 [5].
- UTIA is providing source code for the EdkDSP AMP demo applications and SW projects for the Xilinx SDK Vivado 2015.2 [6]. SW projects are linked with the UTIA library `libwal.a` serving for the EdkDSP communication.
- The evaluation versions of EdkDSP accelerators have HW limitation of the maximal number of performed vector operations. If this limit is reached, board OFF/ON is needed to function again.
- UTIA EdkDSP C compiler is provided as Ubuntu binary utility (use 64 bit Win 7 VMware Workstation 12 Player).
- Partners of the Artemis EMC2 project can get from UTIA the source code for the HW design projects with the evaluation versions of the EdkDSP accelerators in form of AXI-lite netlist pcores free of charge.
- Release version of AMP designs and the EdkDSP package for the Xilinx ZC702 board is offered by UTIA. Customers can order and buy from UTIA the release version of this AMP demo. It includes the source code of HW design projects with the EdkDSP accelerators in form of AXI-lite netlist pcores with no HW limitation of maximal number of performed vector operations.

VII. KEY FEATURES OF THE HDMI DEMOS

HDMI design shows how to interface HDMI output of the TE0701-05 carrier board [3]. See Fig. 1. It requires a monitor

capable of displaying Full HD resolution at 60 frames per second (1080p60); this demo works with fixed video signal 1920x1080p60 (pixel clock is 148.5 MHz). Test pattern generator TPG generates the output image. The TPG pattern is changeable during the runtime. This demo can be executed on Trenc HW [2] and [3] without the FMC IMAGEON card [14].

IM-HDMI design is almost the same as the HDMI design but the video signal from TPG is routed through FMC IMAGEON [14] HDMI output. The demo allows changing video resolution during the runtime thanks to the programmable clock generator on the FMC IMAGEON expansion board [14].

IM-HDMI-HDMI is a video pass through design. Video signal originates from FMC IMAGEON [14] HDMI input then it is stored in the video frame buffer. Video stream continues from the frame buffer and drives the FMC IMAGEON [14] HDMI output. The demo allows changing video resolution during the runtime. In case of the resolution of the input video signal is less than the output resolution, it is displayed the input video signal plus black margin to fill the required output resolution. In case the resolution of the input video signal is greater than the output resolution is required, the output is cropped version of the input video signal.

IM-VITA-HDMI demonstrates interfacing Vita 2000 image sensor [16]. The sensor is connected through LCEDI connector on the FMC IMAGEON expansion card [14]. It provides Full HD (1920x1080) video signal at 60 frames per second. This video signal is stored in the video frame buffer, after that it read from the buffer and displayed on the monitor via FMC IMAGEON HDMI output.

VIII. CONCLUSIONS

Presented enhanced demonstration platforms including basic innovative techniques overview helps to initiate and implement concrete bottom-up collaborations with partners of the EMC2 project.

ACKNOWLEDGEMENT

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