

EMC2

Prototyping and Benchmarking of PikeOS-based and XTRATUM-based systems on LEON4x4

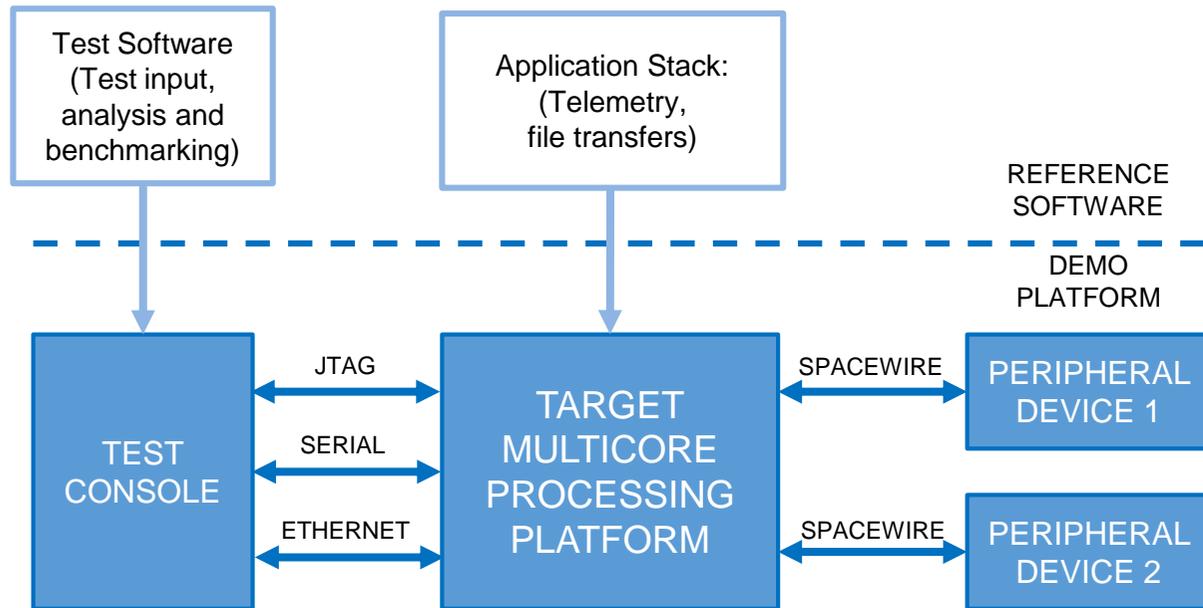
Introduction

- Multi-core architectures will be adopted in the next generations of avionics and aerospace systems.
 - Integrated Modular Avionics (IMA): mixed-criticality
 - Key requirement: spatial and temporal isolation
- Virtualization appears to be a promising technique to implement robust software architectures in multi-core avionics platforms.
 - Goal: exploiting virtualization in the prototyping of a multi-core test platform for the aerospace domain.
- This is a first attempt to exploit paravirtualization on Cobham-Gaisler LEON4, the European Space Agency Next Generation Microprocessor (NGMP).

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Reference Application



- Scenario: various levels of criticality and dependability both at software and hardware level
- Requirements: reliability, robustness.

Overall objectives:

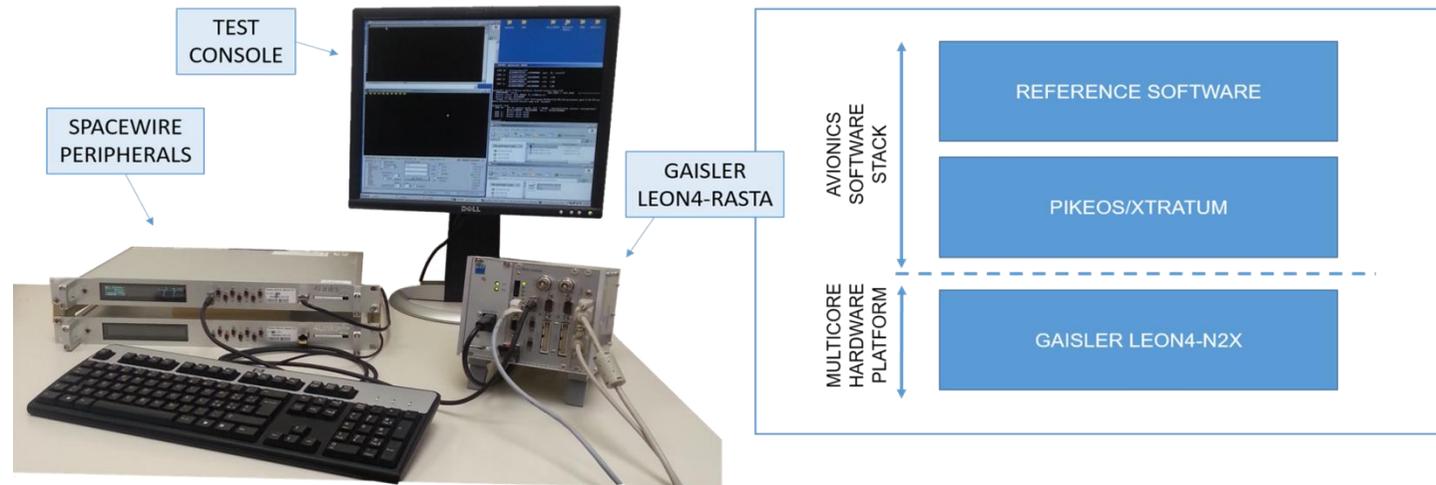
- Implementation and analysis of a typical mixed-critical aerospace application over a next-gen multicore platform
- Assessment and analysis of virtualization technologies (isolation)
- Comparison of different hypervisors (robustness, self-healing)

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Platform & Tools

The target hardware identified is a quad-core architecture based on the Gaisler SPARC-V8 LEON4 processor (ESA's Next Generation MicroProcessor).



Two different hypervisors, SYSGO PikeOS and FentISS XtratuM, have been considered for the implementation of the reference application on selected multicore platform.

pikeOS

- PikeOS is a platform providing RTOS, type I hypervisor and paravirtualization functionalities.

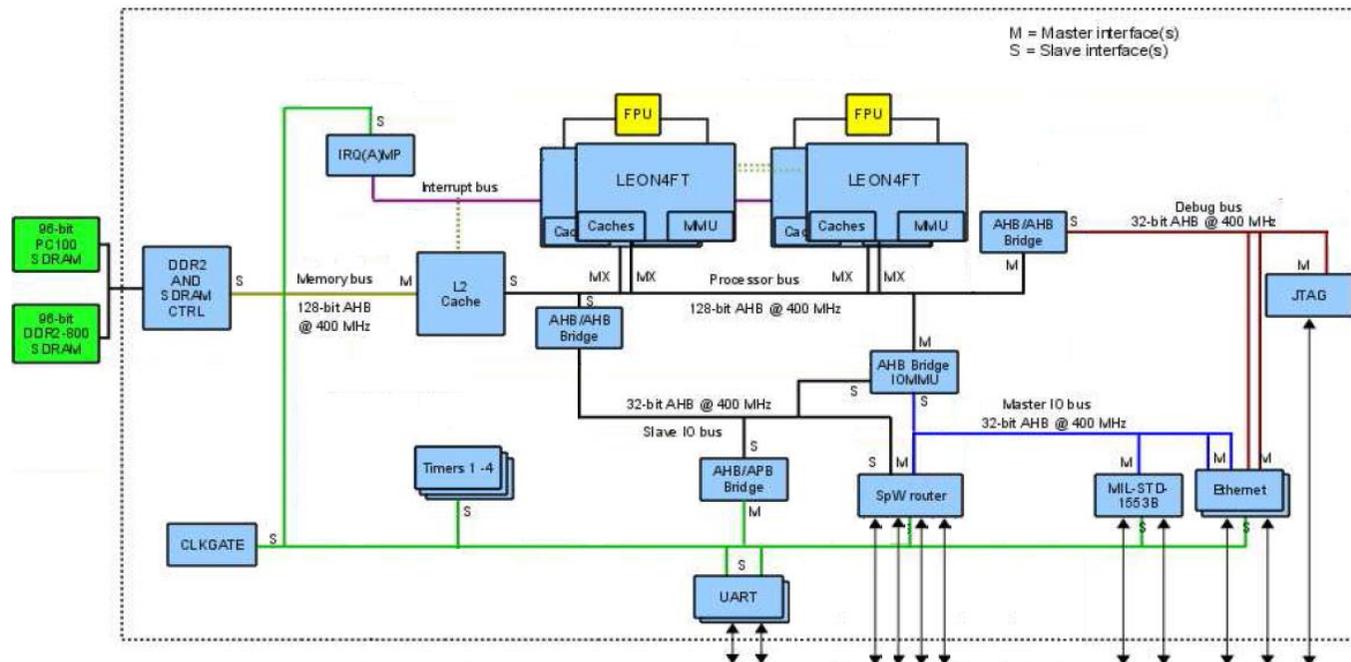
XtratuM

- XtratuM is an open-source, bare metal hypervisor targeting real-time systems and implementing the paravirtualization principle.

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Leon4 Platform

The LEON4-NGMP-DRAFT device is a system-on-chip featuring a quad core fault-tolerant LEON4 SPARC V8 processor having 4x4 KiB instruction and 4x4 KiB data caches



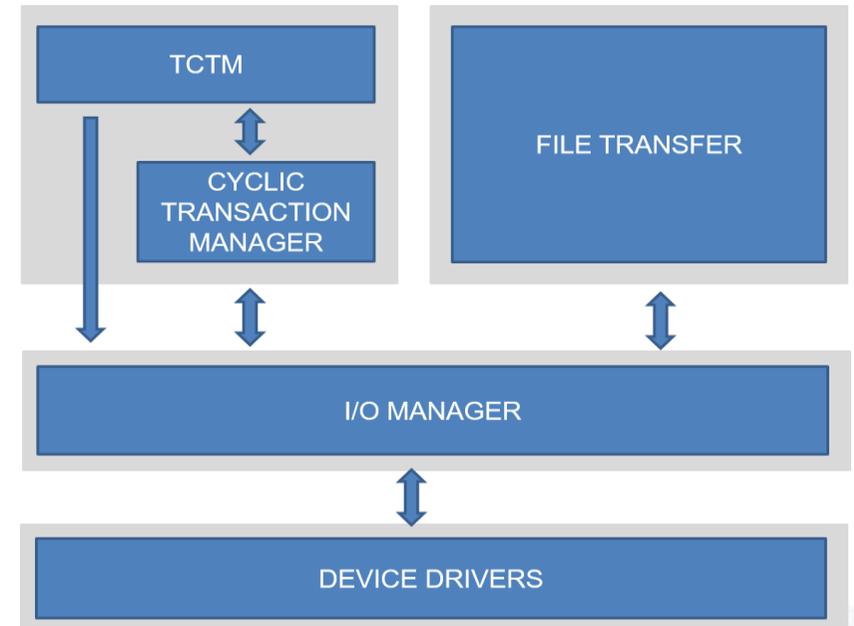
- Double precision IEEE-754 floating point units
- CPU and I/O memory management units
- Multi-processor interrupt controller with support for ASMP and SMP
- 256 KiB Level-2 cache
- SpaceWire router with eight SpaceWire links
- 2x 10/100/1000 Mbit Ethernet interfaces
- MIL-STD-1553B interface
- 2x UART, SPI, Timers and watchdog, 16 pin GPIO
- Advanced on-chip debug support

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Software Architecture

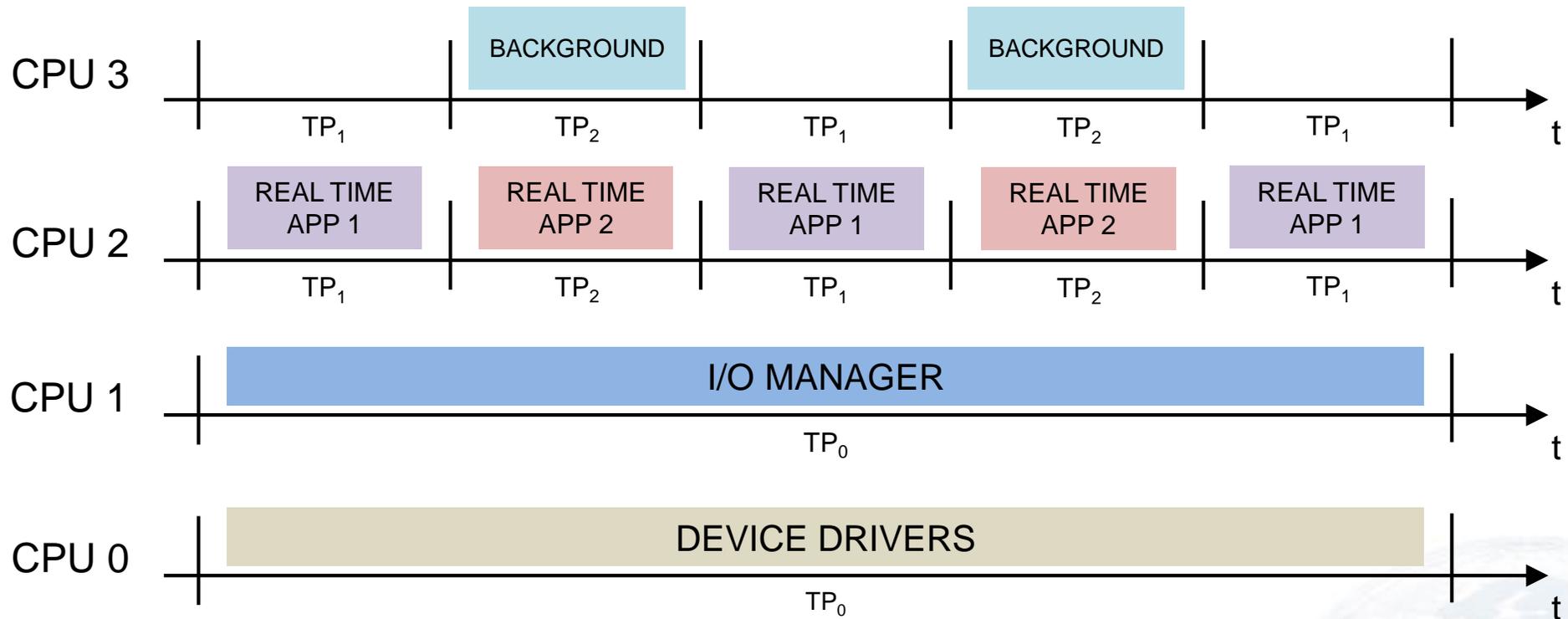
The prototype software architecture includes various components running on top of the hypervisor:

- **Applications**
TCTM, File Transfer
- **Cyclic Transaction Manager**
Packet formatting
- **I/O Manager**
Low level management of data transactions
- **Device Drivers**
UART, SpaceWire, Ethernet



Time and Space Partitioning

Defined software objects have been mapped to separate partitions. The allocation of partitions to different CPUs has been then analyzed, specifically considering functional and timing requirements.

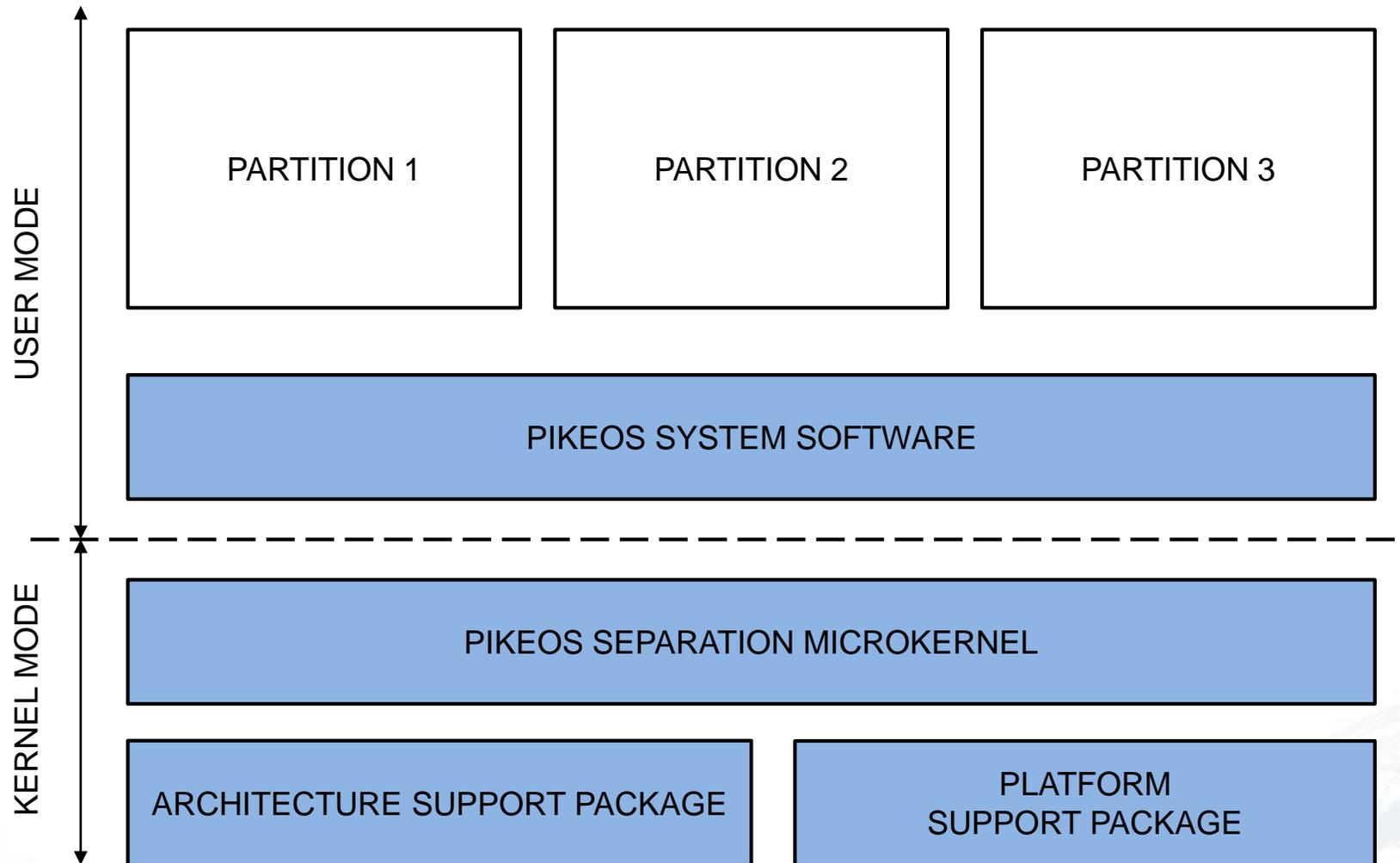


Specific focus has been put in the design of the I/O manager component:

- Mapping of different types of transactions (Cyclic and Sporadic TCTM transactions, File transfers) on different traffic classes
- Definition of scheduling rules for an efficient traffic management

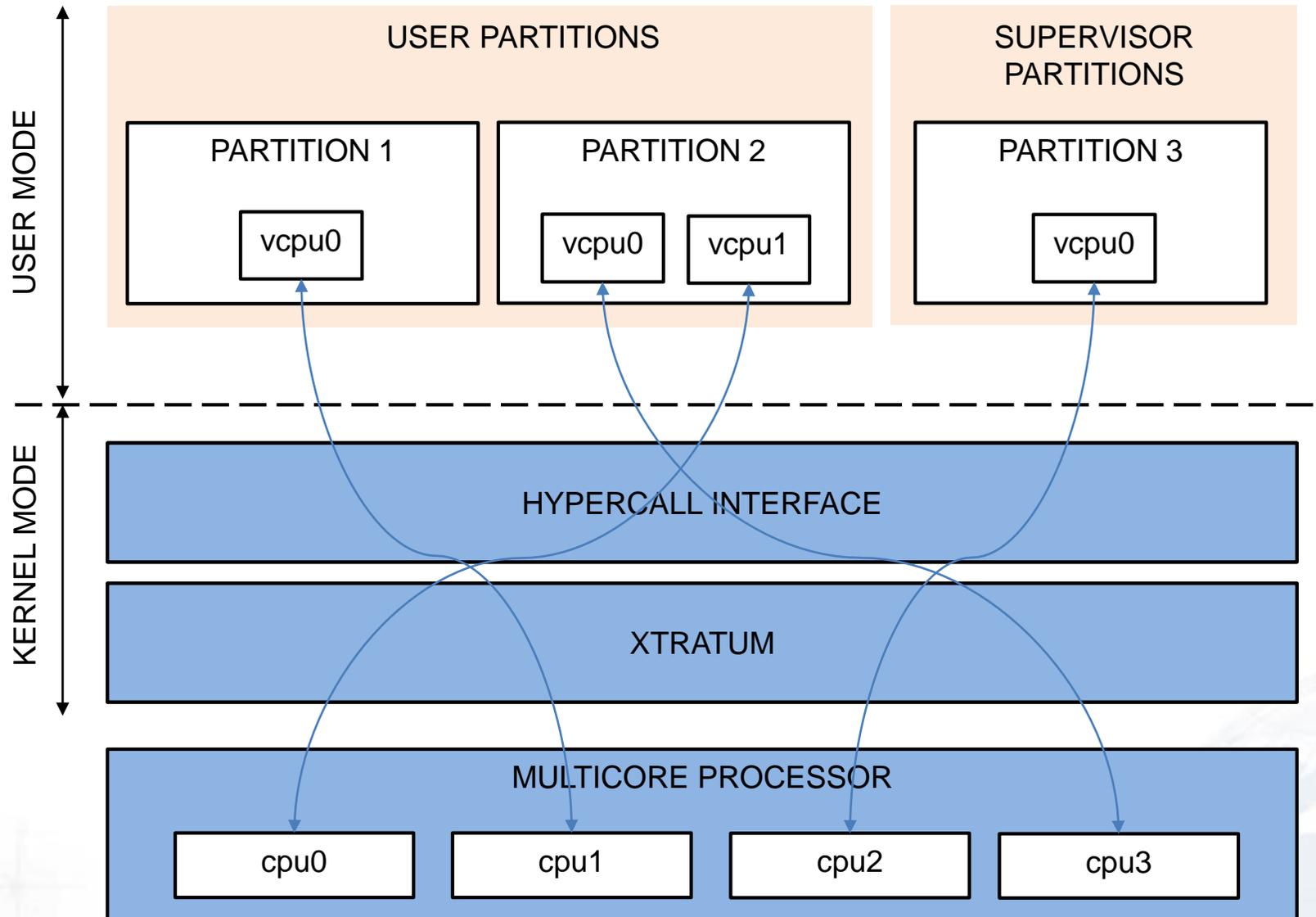
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PikeOS



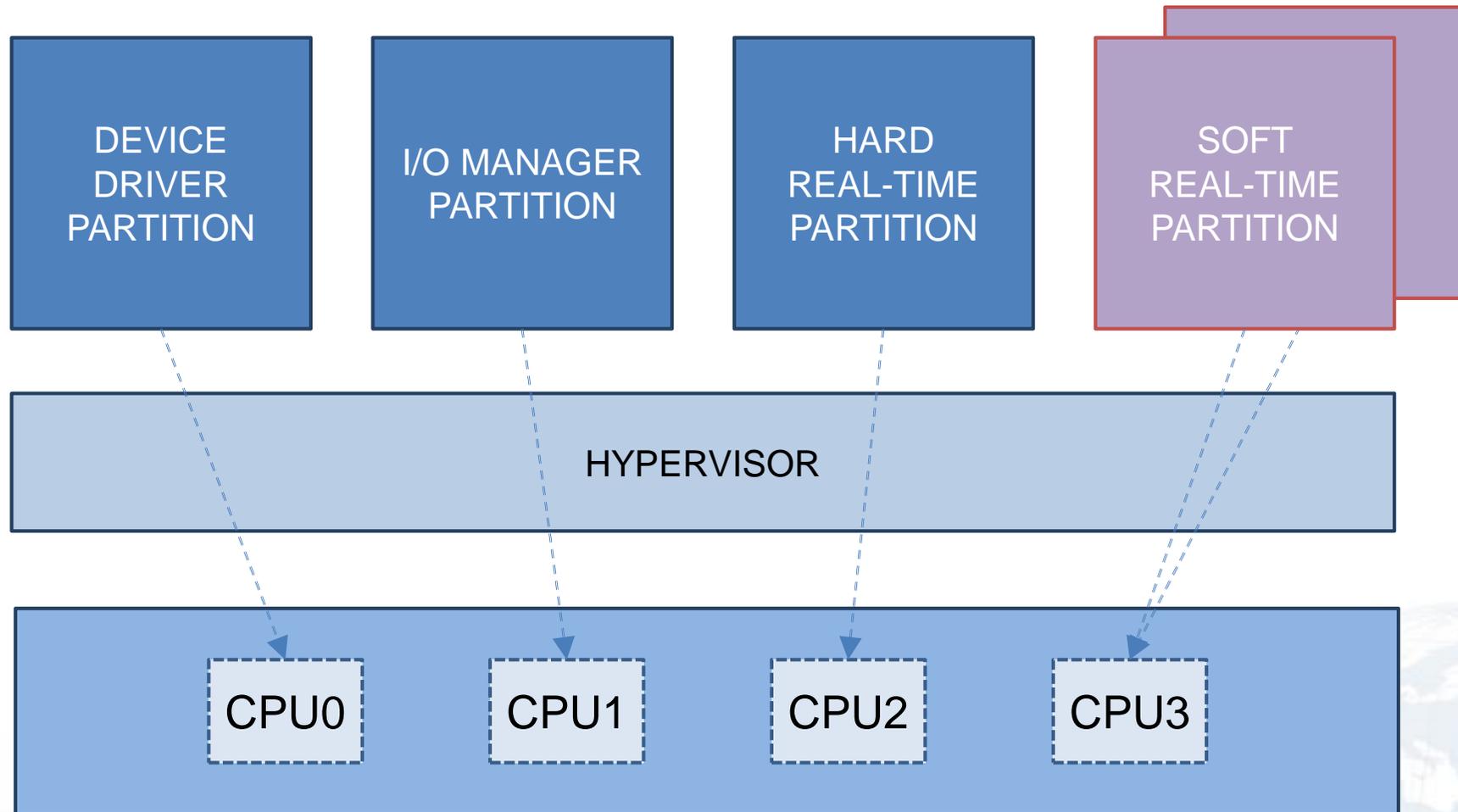
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XtratuM



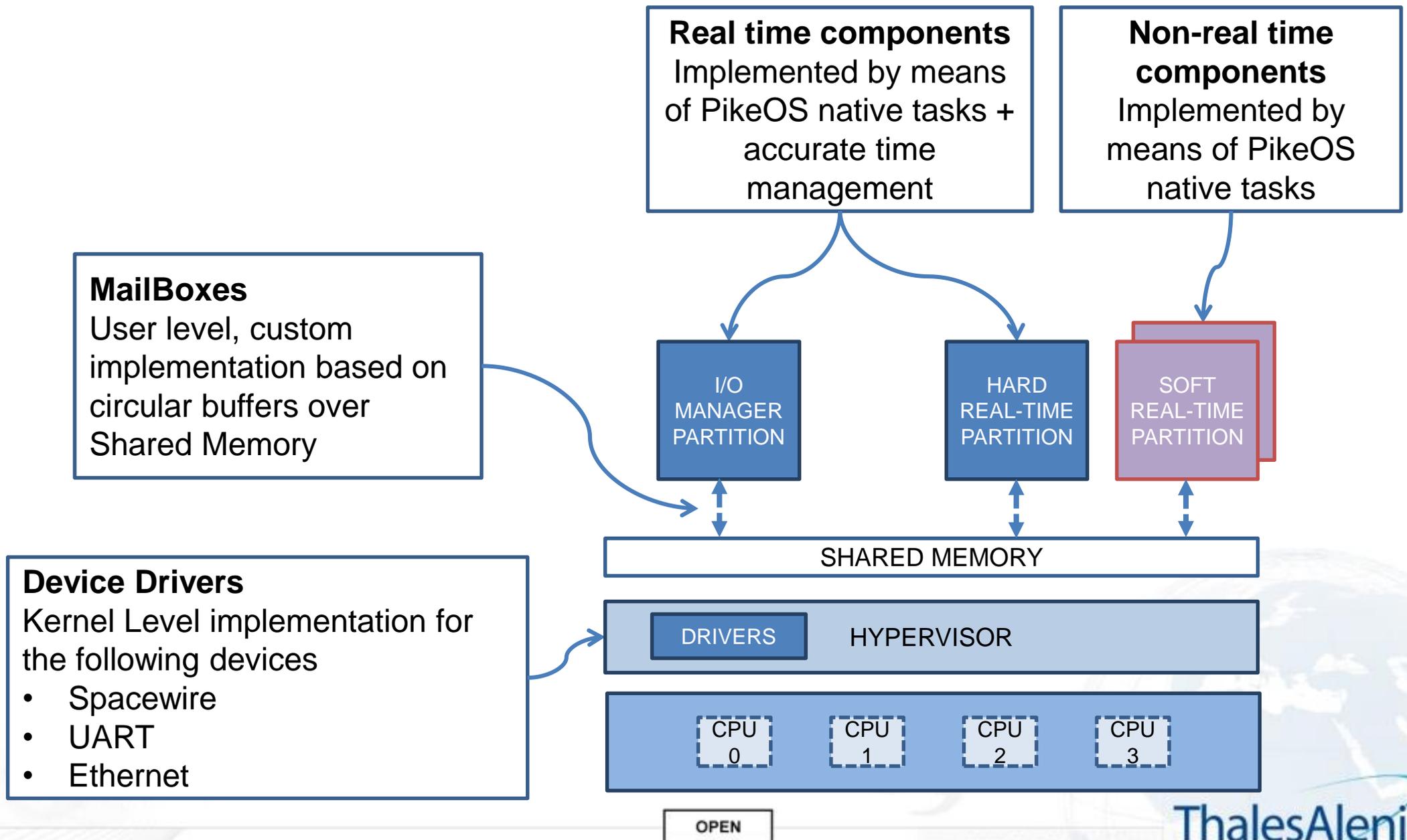
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Partitions and CPU mapping

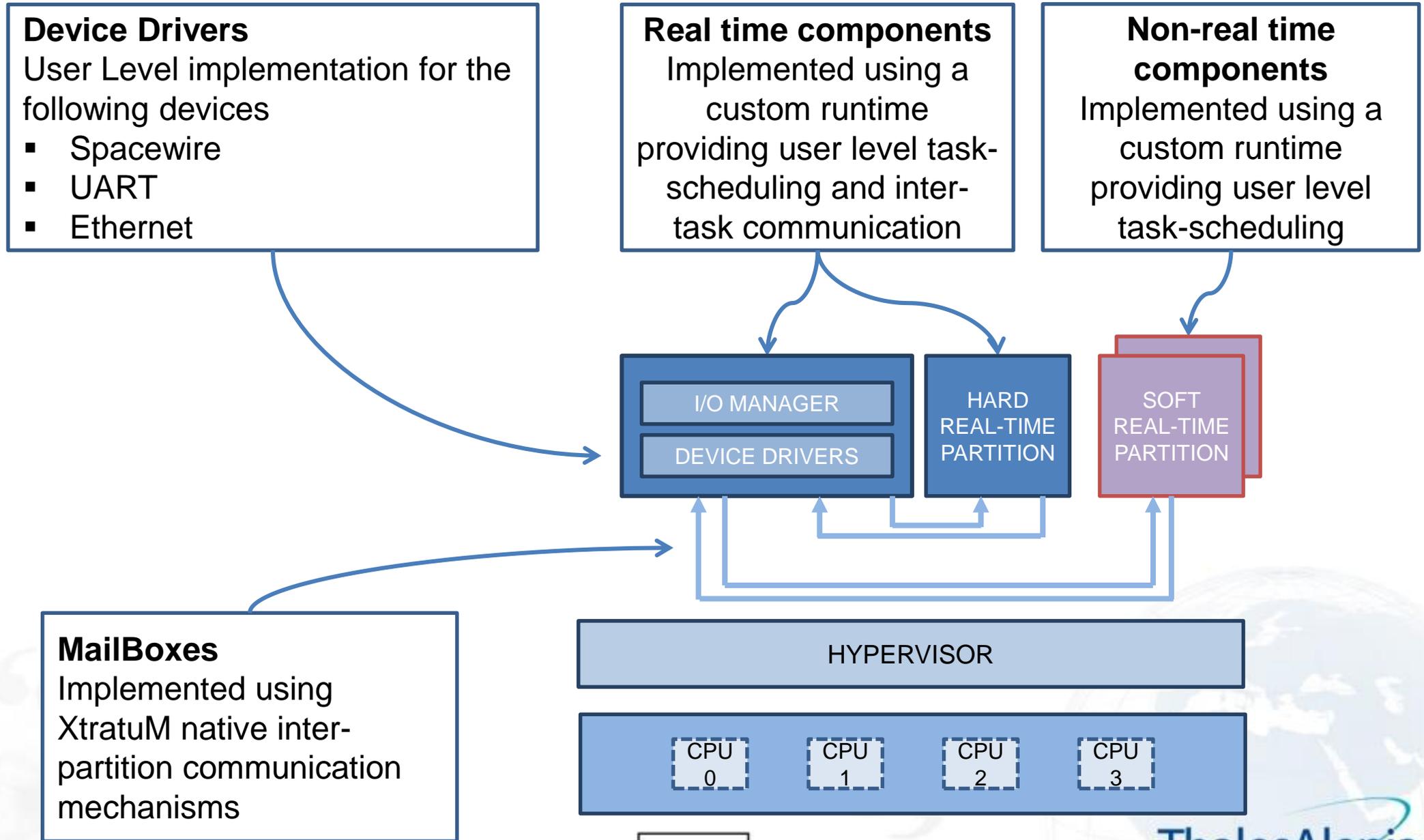


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PikeOS-based application



XtratuM-based application



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