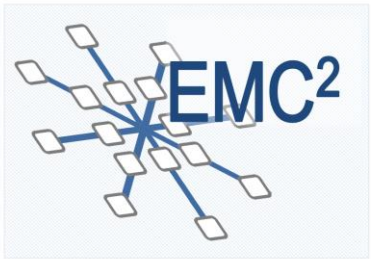

Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments

Project Acronym:

EMC²

Grant agreement no: 621429

Deliverable no. and title	**D5.26 – Requirement Document for AMS Tools and design flow aspects**	
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Publishable Executive Summary

Micro-Controller products (but not limited to these applications) contain more and more analog-mixed-signal (AMS) functionality, which is integrated into one single SoC. These integrated AMS-IPs are becoming the dominant reason for re-spins of the SoC and often cause a delay for market entry.

Figure 1 shows a block-diagram of a "Diesel Direct Injection" application from Infineon with a level of AMS-IP integration.

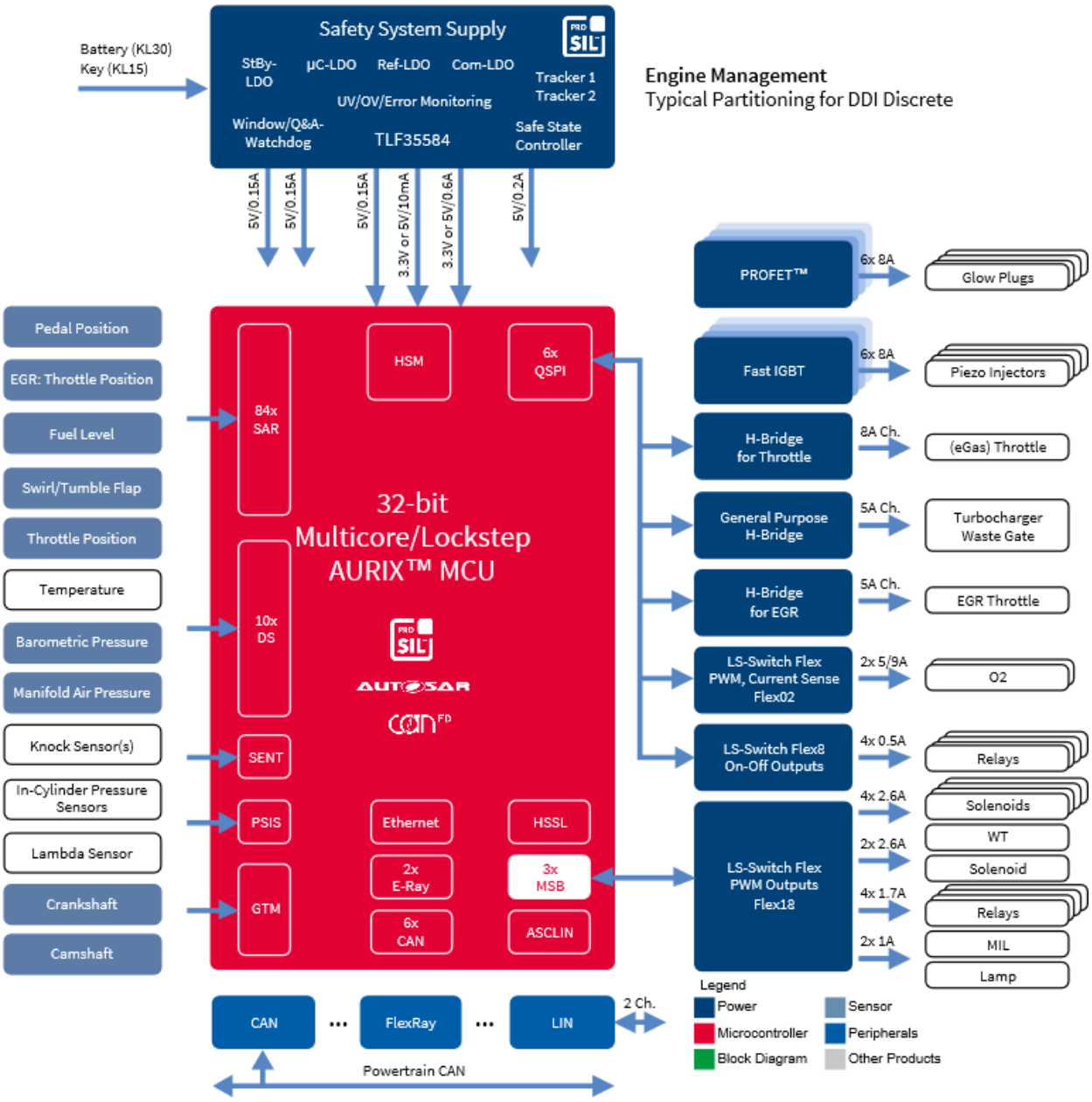

Figure 1: Infineon's "Diesel Direct Injection" SoC with a high level of AMS integration

Many of the problems and inconsistencies of analog functionality integrated into SoCs have the following reasons:

- Today there are still two different design styles and even environments for analog design and digital SoC development. The required transfer of the AMS-IP to SoC-environment requires a

preparation and packaging of the AMS-IP, which results in compromises to be a risk for the correct electrical SoC-integration.

- The integrated AMS-IP cannot be fully verified within the context of the SoC. Although an AMS-IP is working correctly in its isolated environment, this is no guarantee for the full functionality within the SoC.
- Product-Requirements are neither linked to the analog environment nor proper broken down for analog development. Thus, the IP-development is not consequently in the scope of the real Product-requirements but is often based on the experience of the analog designer.

This disconnect between AMS- and SoC-Design (in the phases requirement-engineering and design-environment) leads to inconsistency and major problems on the SoC and is very inefficient in respect to costs, performance and schedule. These problems are becoming even more complex and critical for SoCs with high level of AMS integration.

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1. Introduction

An isolated AMS-IP development with a compromised view generation for SoC integration (as of today) does not reflect the strategies "from Product to System" and "from IP to Product".

Future Design platforms need to support a proper context switch from full-custom to semi-custom and vice versa. This needs to be enabled by new and/or improved design tools and methodologies. In addition, the AMS-IP designer must have the integration into SoC in mind from the beginning on and a well-defined standard interface (from analog to digital) must be part of the AMS specification. This interface block is a digital hierarchical block within the AMS-IP. On the one hand, it must be small enough to allow a full qualification with full-custom methods and on the other hand it has to fulfill all the requirements for the SoC-integration with semi-custom tools (e.g. Automatic Place & Route).

1.1 Objective and scope of the work

We decided to align the Delivery 5.26 to the structure as described in the EMC² Deliverable 5.3 – Integration requirements elicitation template.
The iFEST Platform – industrial Framework for Embedded System Tools, which is a result of an ARTEMIS JU project (REF) is used to address the integration of tools and methods necessary both for an effective AMS-IP development and an efficient and correct SoC integration. This platform grants an open tool-chain

- with the possibility of easy tool exchanges,
- with tools providing services,
- with virtual links, and
- with the system being managed and observed by a specific administration tool – the orchestrator.

The iFEST Platform enables tool replacement and tool independence. Figure 2 shows the iFEST tool framework, where tools are dynamically linked via tool adaptors - TA. The focus with the current task is to develop several additional TAs for existing AMS tools but also to build new tools, based on new requirements, to increase productivity in AMS development and especially with integration of AMS-IPs into a SoC.

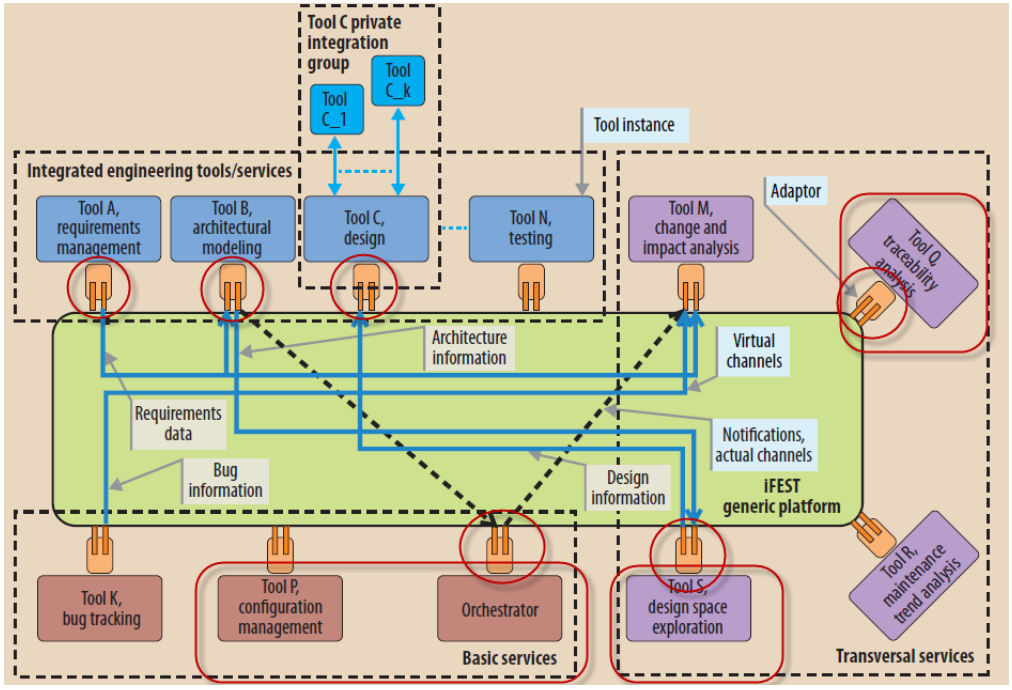

Figure 2: The original iFEST tool platform, showing the development focus points within EMC²

1.2 Structure of the deliverable reports

The intention of this document is to give a short introduction into the challenges with AMS-IP-design and their SoC-integration. To be compliant with the methodology described in D5.3, two additional documents will be delivered:

1. Provide the content for the P&B file (Pain & Benefits, as described in D5.3).
2. Provide the content for the TIM (Tool Integration Matrix, as described in D5.3).

The following tables (Table 1 and Table 2) show an extraction of P&B and TIM related to the SoC-integration of AMS-IPs. They intend to present the basic problems of AMS-IP development and their SoC-integration in detail, which are mainly caused by today's separation of the AMS- and digital SoC design environment.

P&B and TIM are living documents and will be adapted throughout the runtime of EMC^2. A more comprehensive version will be provided with the second deliverable D5.27.

Table 1: Extract of P&B

Phase	Problem	Detailed description	Impact on Effectiveness (Defects)	Impact on Efficiency (Cost)	Importance
Specification & Requirements	Requirements are handled with different tools and formats	no common platform for requirement setting available	requirements need to be transferred individually between the different parties. Inconsistency and/ or not complete set of requirements	Huge rework: - 70% of effort in RE - late rework in D /I of Modules and subsystems because of inconsistency and missing requirements - potential risk for a redesign	H
	no transparent dependencies between requirements, specifications, implementation and documentation	new requirements and change requests need to be manually entered in different docments; no consistency, dependency and transparency given via the differrent documents and down to design and verification	design and/ or verification not complete; final spec and design not consistent; Bugs	huge manual work (30%); high risk of incompatibility and late design changes and/or respins necessary	H
Design	Design-Specification not golden source	Specification is not handled as golden source within the design process	different parties within HW, SW, Verification and Validation need to transfer information manually for their design task => errors, missing details, inconsistency	a lot of effort for debugging and rework need to be spent in HW, SW, Ver and Val in a very late state of the design process and even silicon (re-spin)	H
	Manual transfer of design parts from owner ot SoC	SoC-design comprises of different tasks in different groups on different locations; to guarantee the consistency of the different parts of the design is manually checked and errorneous.	to guarantee the consistency of the different parts of the design is manually checked and errorneous. This procedure is not compatible with ISO26262	a lot off effort for manually checks and redelivery because of inconsistency of Ips, Subsystems, libraries, … not conform witj IO-requirements	H

Table 2: Extract of TIM "user stories"

	IFX AMS Tool matrix							Filter options			
Section 2			Development phase				Development phase	NONE		Filter	Add a new row
US	Prio	Status	from...	Tool A	Output	Format	to...	Tool B	Name: Purpose	Description	Actors
1	1	Approved	RE&A	Req-Cap	request	*	*	Rel-Mgr	Req-Cap: Requirements are enterdéd into a common Design Database.	Activities in Tool A: SoC-Requiements are captured and enterd via Req-Cap into a common DB. Now requirements can be handeled via a dedicated Requirement process Req-Pro Exchange description: Data are stored within Rel-Mgr Activities in Tool B: provides a new release of the requirements and give a notice	Tool A User System-/ Concept engineer Tool B User System-/ Concept-/ Design-engineer
2	1	Approved	*	Rel-Mgr	request	*	V&V	Asure	V-Plan: Requirements already in the Databas are used to set up the verification plan of an AMS-IP together with design- and concept engineer	Activities in Tool A: gives a notice that new data are available Activities in Tool B: Requirements are used for defining a verification tasks/ plan for an AMS-Function/ IP on different levels (IP, Subsystem, SoC, validation)	Tool A User Verification Engineer, Concept engineer Tool B User Verifiaction engineer
3	1	Submitted	V&V	Asure	file	*	V&V	SIM-M	V-Track: Each entry in the Asure-DB (Verification-item) is linked via V-Mgr to the simulation results	Activities in Tool A: provides the relevant feature, which need to be verified on IP level Activities in Tool B: Mapping of implemented simulation cases to features within the verification plan	Tool A User Verification Engineer, Concept Engineer Tool B User Verification Engineer

2. Development and SoC-Integration of AMS-IP (State of practice)

2.1 IP development and verification

The AMS IP development is mainly done in parallel to the product design, but, as mentioned earlier, in a different and isolated design environment. With preparation of the AMS-IP and the transfer from full-custom to the semi-custom environment important information is not available or gets lost due to insufficient tools.

E.g. for physical integration (P&R) into the SoC only a black-box of AMS-IP is delivered, which shows the area, the pinning, and the interface – timing only. This information is not enough anymore for today's nano-technologies.

The concentration on the development and simulation of the AMS-IP itself is not sufficient, as the SoC-integration may show different electrical conditions, which may not fit with the assumptions made during AMS-IP design and thus the analog behavior within the SoC could run out of specification.

In parallel it is always hard to break down the related requirements for a product to IP-development. There is only a formal link to the Product Requirements Definition via single engineers and the AMS-IP performance is mainly driven out of the experience of AMS specialists. However, not only the IP-design has nearly no link to the PRD but also simulation is not done according to the real customer requirements.

Both together hide a big risk for either Over-Engineering or not fulfilling customer requirements. Over-Engineering results in a more complex IP, costs more area, reduces the product margin and puts a higher risk for a redesign of the SoC.

Modelling of AMS-IPs for functional and electrical verification on SoC-level is a very important component of an IP-delivery. Although an analog behavioral model for functional SoC simulation is provided, there is no proper way to generate these simulation models and to check against the real design. Electrical models to analyze the influence of the SoC to the analog behavior do not exist today.

All misbehaviors from above mentioned weaknesses will be detected on first silicon earliest or even later at the customer.

2.2 Silicon validation

In contrary to pure digital IPs, where a pre-silicon functional verification already reaches a high level of quality and a first time right is within scope, silicon validation for AMS-IPs is still a must in the overall verification strategy. The strong influence of the surroundings of an AMS-block within a SoC, which cannot be detected with pre-silicon measures today, a re-spin of the SoC is very likely and in worst cases even a re-design of the AMS-IP has to be done.

As the test programs will not be tested before silicon is available, the validation progress is delayed due to time consuming debug activities for the test program itself.

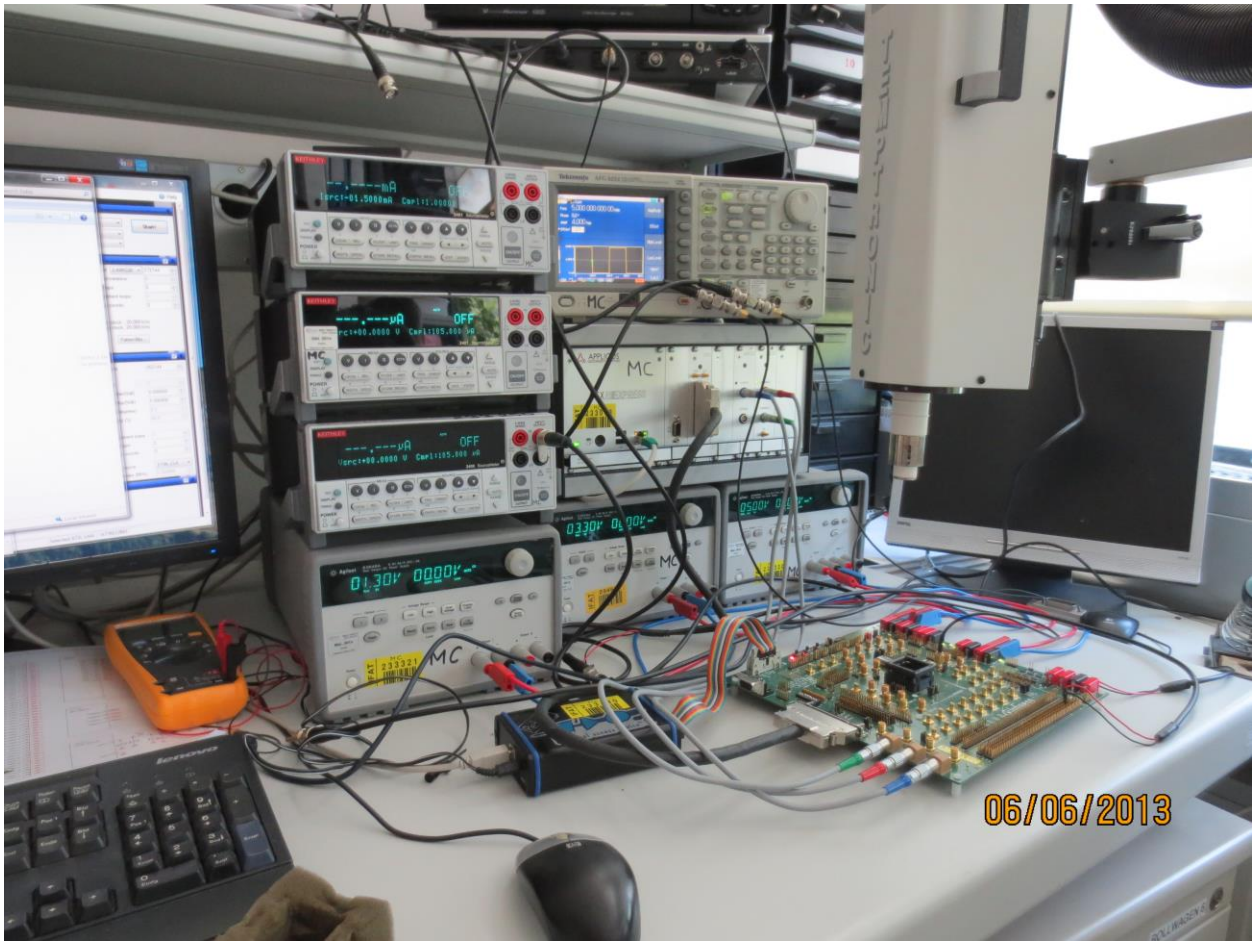

Figure 3: Validation Board and Measuring-Equipment (Example of an AMS laboratory measuring station)

The missing link of silicon validation to product-spec and pre-silicon simulation poses a risk for validation without gaps.

Developing and debugging test-cases in the lab in a very late stage of the product development cycle is very time-consuming and poses high risk for the quality of deliverables due to high pressure of the customer to get first samples.

3. Solution – AMS to SoC-Designflow and Tools

With the extension of the System platform we want to achieve a tight context switch between FC- and SC-Flow. All relevant development data need to be available and fed into a special service to prepare all of the views necessary for a "state of the art" high quality SoC integration.

A link between product requirement and analog design must be implemented to guarantee a requirement-driven AMS design and verification. In addition, high quality and correct AMS-IP models need to be available which allow a successful integration both, from a functional and an electrical point of view.

3.1 Targeted Infrastructure

Infrastructure is an iFEST-like design platform, which will take care for a proper data-exchange between the tools of both, full-custom and semi-custom environments. All tools will be linked to the common platform in a way that the context for IP-design and SoC-integration can be prepared and exchanged easily. The already existing iFest platform offers an ideal base to have analog-mixed-signal and digital SoC tools and methods in one overall design environment from Requirement-Engineering to life-cycle support. New tools necessary to exchange sufficient and consistent information in both directions (e.g. for SoC-Integration, analog re-simulation after integration) can easily be included and are a pre-requisite for a smart and efficient co-design of AMS-IP and SoC design.

The focus in the current project is to develop several such TAs for existing tools, but also to build additional tools or services based on the project development (especially AMS-IP).

3.1.1 Elements of the platform

A Platform-Manager is required as the supervisor for the content of the design system in terms of tool instances at a given moment, PDKs, Libraries, Product-Specs and respective services offered to the platform. The Platform-Manager receives messages from tools, such as notifications, versioning updates, document (links), etc. It then forwards notifications to registered tools and services to initiate the respective update. The Platform-Manager takes care for releases of Specifications, IPs, Subsystem, and SoC-Integration to guarantee the consistency of all data necessary for product-development at a certain design step.

The tools of the platform need to have access to a repository as a physical storage location (to store files released by any or all of the tools interfacing with the platform). This may actually be a distributed physical solution but it is transparent to the user of the framework. The repository is also identified as the "project disk". Each tool and/or user which/who operates on this disk has a private space, which is not public in the project unless it is released.

Tools of both full-custom- and semi-custom-environments must have tool adapters via which they connect to the platform and exchange information in both directions necessary to integrate and design AMS-IPs on a high level of QoR (Quality of Results).

3.1.2 Tools of the platform

An IPGW-IP-Gateway is required to collect all the data coming from the AMS-development. It provides formal checks regarding their correctness and builds a package which includes, besides all necessary views for SoC-integration, a next generation timing model (Glassbox, ILM, Block-Abstract).

A SIMM- Simulation Manager has to support a tight link of product requirements to an AMS-Simulation plan and checks the progress of AMS-simulation with analyzing the results of AMS simulation tools.

MGen, a Model-Generator, should provide a methodology and supports creating the behavior- and the electrical model of an AMS-IP based on product requirements/specifications.

SOC2AMS – An Extraction of all the relevant electrical parameters of the AMS-IP surroundings within the SoC is needed for a final AMS-simulation to finally analyze the impact of the SoC on the AMS-functionality.

3.2 Product-Requirements and AMS-IP Development / Simulation

As mentioned earlier, the full-custom and semi-custom environments are not tightly linked by default to exchange necessary data urgently required for a real AMS-/ SoC- Co-design. The purpose of this work is to get closer to an integrated framework.

But even one step above the link of system related requirements, which are in some cases linked to SoC-Flow to support functional verification and design, a link to the AMS-Environment is currently not available, at least not as a defined standard.

Mapping of System-requirements directly to AMS-IP development is a must to guarantee an effective and efficient IP-development. In today's practice we see an over-engineering of the IPs in many cases to not fail on system-level. But this over-engineering does not pay out, as it is a waste of area and power dissipation in many cases. The higher complexity even puts an additional high risk for a re-design to the SoC. A tight link of System-Requirements to AMS-Design would enable both, a robust IP-development and object oriented measureable simulation.

Last, the integration of an AMS-IP into SoC will only be successful, if there is a functional equivalent behavior-model of the analog block, which will be used for system-simulation (based on use cases) on SoC-level. In tight co-operation with EDA a methodology needs to be established, which supports generating reliable behavior-models of AMS-IPs in terms of equivalence to the real design.

To map the system-requirements for analog parameters for an AMS-IP design (without over-engineering), an electrical-model besides the behavior-model is urgently required. Even if an AMS-IP is working on an IP-level, this will not guarantee the functionality in the same manner after integration on SoC-level. An electrical model to analyze the electrical influence of the SoC on the critical parameter of the AMS-IP (e.g. IR-drop, cross-talk, shielding, ground-bounce, reference voltage, …) in an early stage is becoming the key. Such a model will help to adapt the analog related system-requirements and thus enables an effective robust AMS-IP design.

3.3 IP-Preparation, Modelling and SoC-Integration

The key for proper preparation of AMS-IPs to deliver the right context for SoC-Integration via the common platform is the right architecture of the AMS-IP itself. A structure is needed, which allows a seamless analog design and a SoC-integration. All analog-related circuits must be qualified with analog sign-off. For SoC-integration all signals must be traceable to their endpoint or from their starting points (GlassBox, ILM, BLA) and timing sign-off will be performed on a semi-custom basis. An AMS-IP structure must guarantee a seamless physical SoC-integration.

Figure 4 is a proposal for an AMS-IP structure, which clearly separates the asynchronous analog and the synchronous digital behavior.

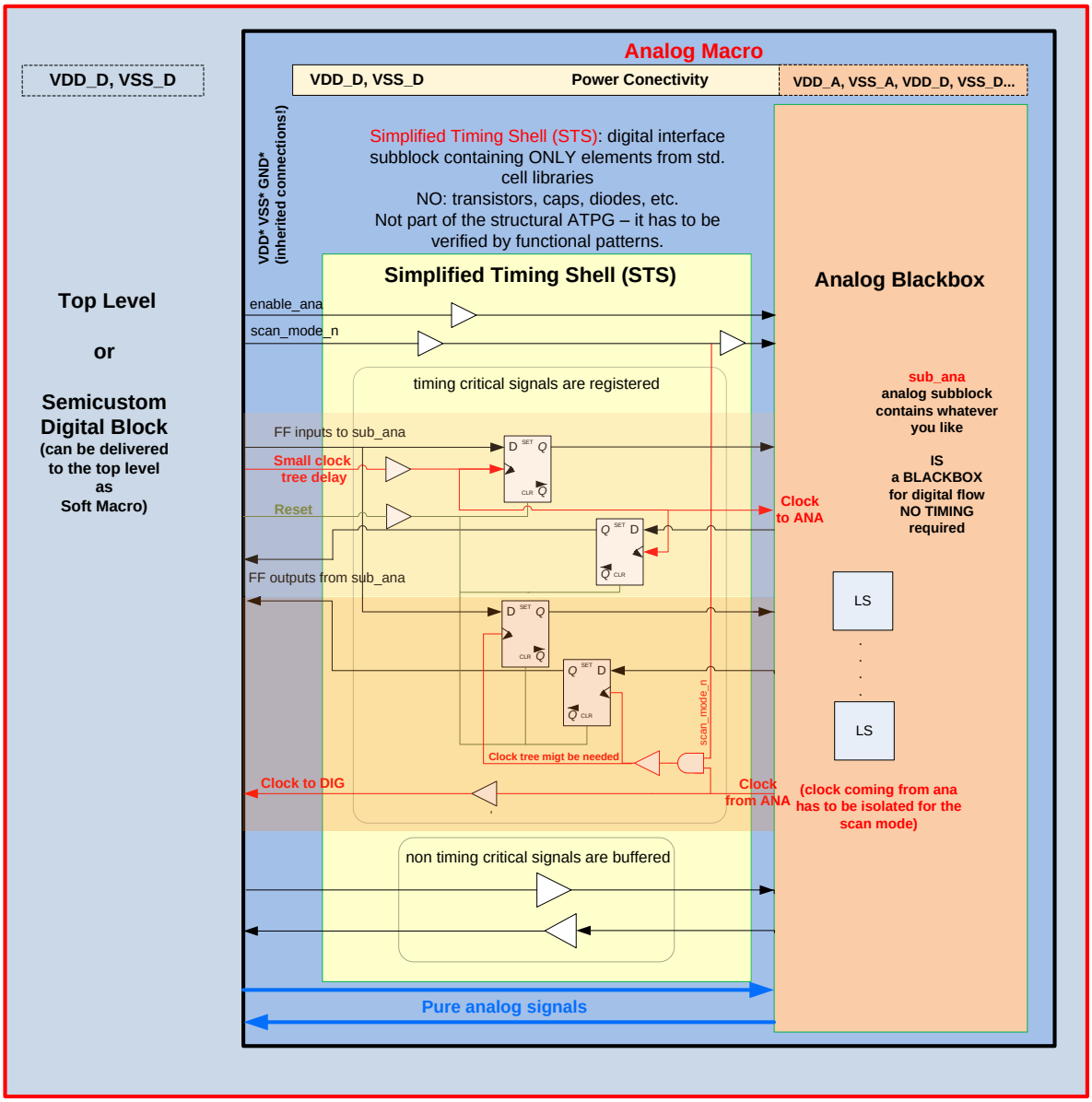

Figure 4: Simplified Timing Shell as the ana-dig interface

The new structure of the AMS-IP consists of two blocks:

- A Simplified Timing Shell (STS):
  - is the interface between analog and digital sub blocks of the macro or between the analog macro and the SoC,
  - should be defined in the design concept phase already,
  - contains only standard cells, which are fully characterized library elements,
  - static signals are buffered,
  - timing critical signals are registered (FFs), and
  - final SoC-level STA will include the digital logic of the STS.

- The Analog black-box:
  - The analog sub block contains all other cells and devices like resistors, transistors, caps, etc.
  - Also characterized cells are allowed in the analog sub block but they will not be tested in the final top level STA.
  - Level shifter cells are part of the Analog black-box.
  - Timing between this black-box and the STS is to be ensured with the analog simulations.

3.4 Strong Link between Pre-silicon Verification and Silicon-Validation

The continuously increasing integration of functionality raises the burden on verification engineers of complex System on Chips (SoCs). Simulations and formal verification alone are not able to detect all problems in a design due to unforeseen interactions between modules and/or the SoC itself.

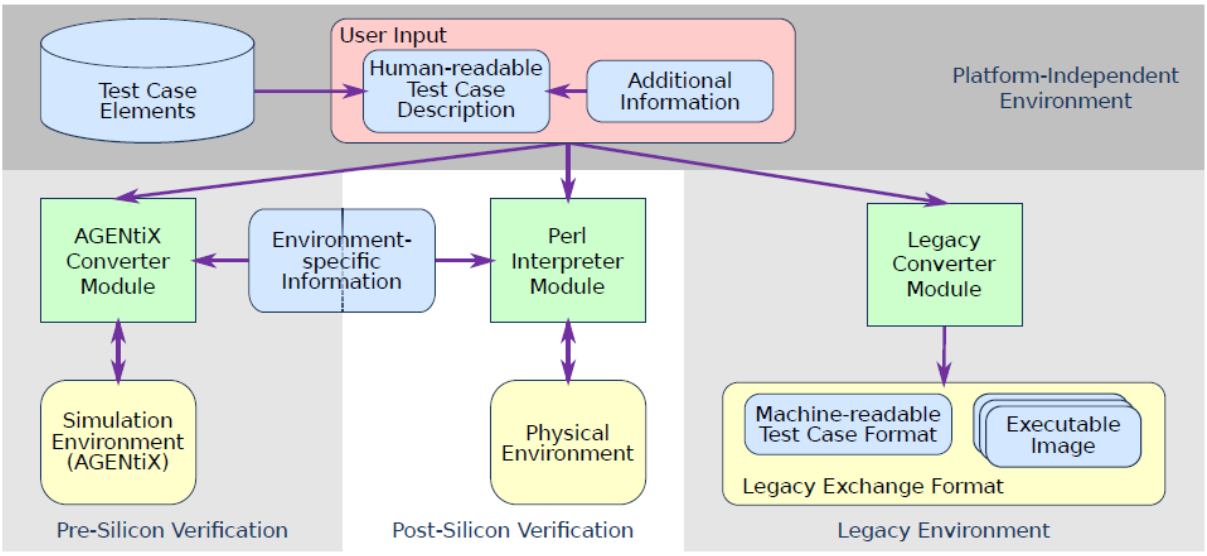

Figure 5: Concept to link Pre-Silicon Verification and Silicon Validation

These problems may occur even if the modules are logically independent from each other due to physical effects. On the other hand bugs found in silicon verification in the laboratory need to be investigated and fixed with the help of design engineers. Therefore, collaboration between pre-silicon and silicon verification is mandatory which further allows raising synergies. Unfortunately, many environments currently in use handle these activities almost in complete separation which complicates co-operations.

A new approach to improve the situation by using a common test description language for pre-silicon and silicon verification is necessary. It allows preparing and debugging test cases with pre-silicon simulation already. This reduces the effort on silicon validation as time can be spent to debug real AMS issues, instead of the test case itself.

3.5 Analog Superblock Multi-ADC

The Multi-ADC is an AMS Superblock, which consists of 30 and more ADCs to be integrated into the SoC. Although the different ADCs are developed due to the requirements described above, there is still a need (analog routing, special structure of power supply distribution, X-talk, shielding, ground bounce) to implement this superblock in a full-custom environment and carry it through all the procedures necessary to transfer an AMS-block to the SoC.

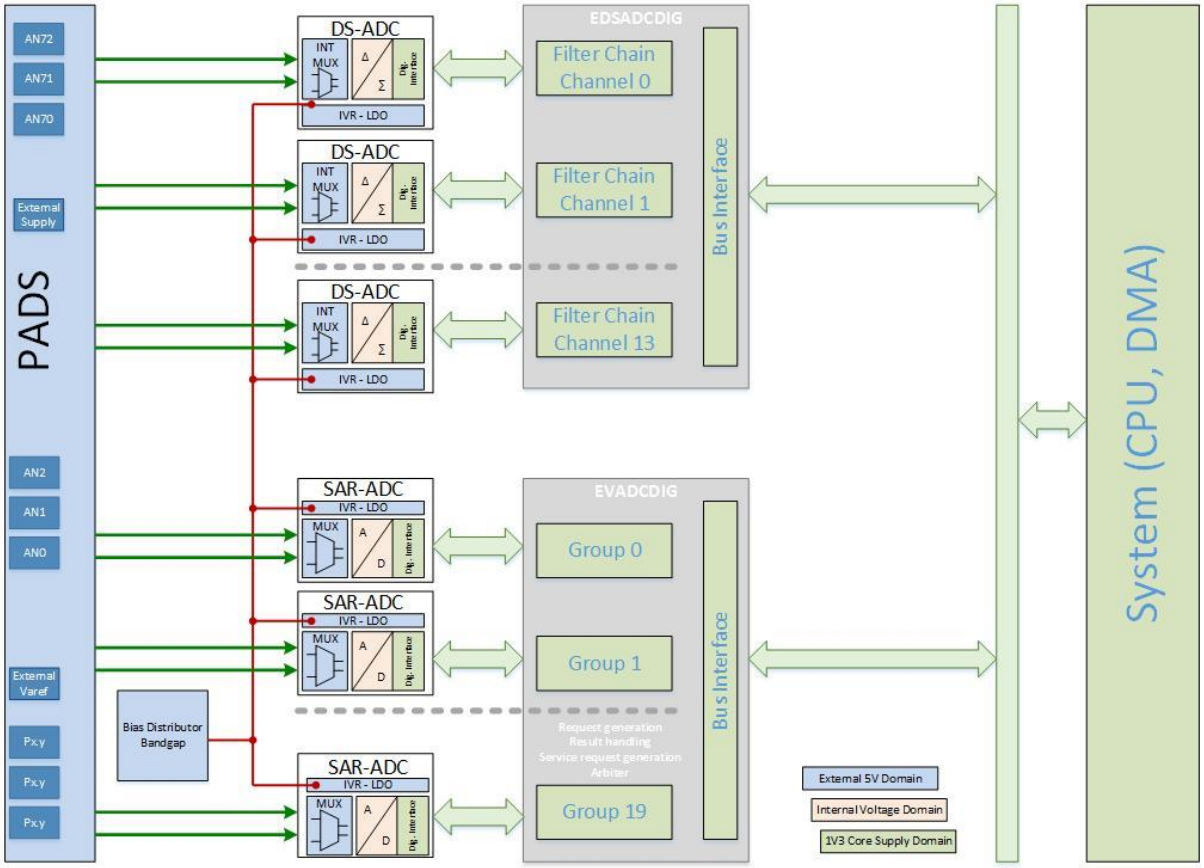

Figure 6: Architecture of the AMS-Superblock Multi-ADC

The AMS design and layout are still processed with the „full custom"-design method. However, the high Time-To-Market pressure requires a shorter development time while, at the same time, providing a higher integration density and maintaining a consistent quality in terms of analog as well as digital function blocks of modern microprocessors. Thus, a "concurrent engineering" model is implied which entails an increased complexity in the existing methodology of common integration of the analog and digital functionality.

One significant challenge in this project is, among others, to bring together the digital methodologies with the analog world. Moreover, the analog boundary conditions need to be defined in a way so that the advantages of the digital automation, which are already established for many years, are harnessed for an analog circuit design. This results in a significant increase in efficiency on system-integration-level of the analog part. An additional result is the higher productivity in the analog physical design which particularly occurs during change requests and within product-families while, at the same time, the required high quality standards are maintained.

Implementing the M-ADC with semi-custom automatic Place & Route grants reproducibility and reuse for product derivatives. In addition, the required AMS preparation for integration is not necessary anymore, as the layout already contains the right information. This means that no transfer from a full-custom to a semi-custom environment is required.

4. Conclusion

A tight interaction of AMS-design and SoC-development within one common System-Design Environment in respect to AMS-IP SoC-integration and requirement handling is the key factor for further productivity gain and an improved quality for complex SoCs. Time to Market will be reduced due to less re-designs and/or even late detection of AMS weaknesses on the customer-side.

The present deliverable is only an initial version of a more covering activity plan of requirements for a common and tightly linked platform both to gain a high productivity of AMS-integration and to reach a high level of QoR for integrated AMS-functionality even before first silicon.

Thus, not all of the addressed tools and services are considered within the current deliverable and more tools and functionalities are expected to be covered. The supporting P&B and TIM files are "living documents" until the end of the EMC^2-project.

A second delivery summarizing the still ongoing activities is planned to be submitted in M24.

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[1] EMC² Deliverable 5.3 - Integration requirements elicitation template.
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6. Abbreviations

Table 3: Abbreviations

Abbreviation	Meaning
µC	Micro-Controller
ADC	Analog to Digital Converter
AMS	Analog-Mixed-Signal
AMS-IP	Analog-Mixed-Signal Intellectual Property
BoM	Reduced Bill of Material
EDA	Electronic Design Automation
EMC²	Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments
FC	Full-Custom
iFEST	industrial Framework for Embedded Systems Tools
IPGW	IP-GateWay
MGen	The Model-Generator
P&B	Pain & Benefits
PRD	Product Requirement Definition
QoR	Quality of Results
SC	Semi-Custom
SIMM	Simulation Manager
SoC	System on Chip
STA	Statix Timing Analysis
STS	Simplified Timing Shell
TA	Tool adaptor
TIM	Tool Integration Matrix