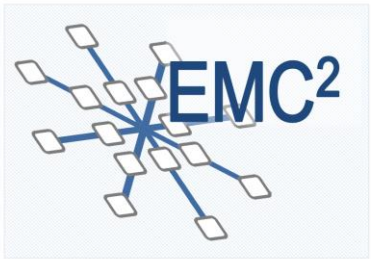

Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments

Project Acronym:

EMC²

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Publishable Executive Summary

Embedded systems are the key innovation driver to improve almost all mechatronic products with cheaper and even new functionalities. Furthermore, they strongly support today's information society as inter-system communication enabler.

Consequently, boundaries of application domains are alleviated and ad-hoc connections and inter-operability play an increasing role. At the same time, multi-core and many-core computing platforms are becoming available on the market promising a breakthrough for system (and application) integration, efficiency and performance.

A major industrial challenge arises from the need to face cost efficient integration of different applications with different levels of safety and security on a single computing platform in an open context.

The objective of the EMC² project (Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments) is to foster these changes through an innovative and sustainable service-oriented architecture approach for mixed criticality applications in dynamic and changeable real-time environments.

In a first step to achieving the goals set in this direction by the EMC^2 WP 4 partners, this document provides the requirements for the EMC^2 technology work package WP 4 work. The captured requirements are derived from the high level (HL) requirements document developed in WP 1 and also make reference to these HL requirements. Based on the requirements derived in WP 4, the WP 4 partners will focus on developing hardware and software supporting the needs of embedded, mixed-criticality multi core systems. WP 4 has analyzed various predecessor projects investigating various different approaches for platforms that can provide such features and functionalities. It is the aim to combine the best results from these predecessor projects and make add-on developments for optimization. The development results will aim at satisfying next generation product-needs of the automotive industrial domain. These are strongly oriented towards safety applications up to Advanced Diver Assistance Systems (ADAS) and highly automated driving functions.

The document provides an overview on previous and other running European Commission funded research projects forming the basis of developments planned in WP 4. The captured requirements are attached to the document in the annex. The requirements are inserted into an EXCEL template capable of being read by the DOORS requirements management tool for potential processing if required.

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1. Introduction

1.1 Objective and scope of the document

This document forms the basis for the development planned in EMC^2 WP 4. It defined the derived WP 4 requirements needed for the hardware and software developments due in EMC^2 WP 4. WP 4 builds on the results of other European Commission funded projects. This document briefly summarizes these projects and in this way constitutes the "state of the art" at the beginning of the EMC^2 project in the subject field of work.

1.2 Structure of the deliverable report

The first part of the document will briefly provide the reference projects that form the basis of the work to be conducted in EMC^2 WP 4. The requirements are based on the WP 1 "high level requirements" and are defined in the EXCEL sheet attached to this document in the annex.

2. Related European Funded Projects

2.1 GENESYS

GENESYS was a European FP 7 research project in 2008 and 2009. During this project a cross-domain reference architecture for embedded systems was developed.

2.1.1 Overview

The development has been driven by following three challenges:

- complexity management – systems are ever-increasing in cognitive complexity;
- robustness – a system must deliver an acceptable level of service even in presence of faults;
- energy efficiency, which became very important due to the growth of the market of mobile devices.

With GENESYS a composable, robust and comprehensible component-based framework has been established. The architecture separates the computation from message-based communication and ensures a deterministic and timely transport of messages.

2.1.2 Service-oriented Architecture (SoA)

A service-oriented architecture is a design pattern based on software parts providing a specific functionality as a service to other applications. The GENESYS architecture provides a minimal set of core services, i.e. mandatory services which offer mechanisms to compose a system, e.g. basic configuration and communication services. Furthermore, several optional services, e.g. diagnostics and security, have been defined.

2.1.3 Prototype

During the project a prototype for the industrial domain has been constructed. The main part is a Time-Triggered Network-on-Chip (TTNoC) serving the interconnection between possibly heterogeneous IP cores (called micro components). Each micro component running a specific application and is connected over a Trusted Interface Subsystem (TISS) to the TTNoC.

The structure of the prototype is depicted in Figure 1. Two micro components, the Trusted Resource Manager and the Resource Management Authority, implement optional services of the GENESYS architecture (namely resource management and reconfiguration).

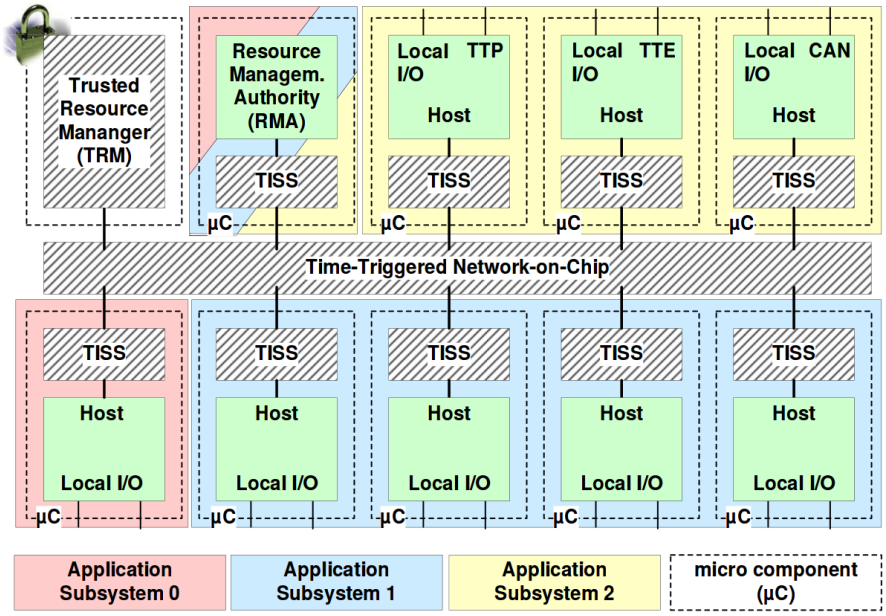

Figure 1: Overall structure of the GENESYS prototype.

2.1.4 Deterministic Networking

A system behaves deterministically if and only if, given a full set of initial conditions (the initial state) at the initial instant, and a sequence of future timed inputs, the outputs at any future instant t are entailed [2].

The deterministic and timely transport of messages is established by the TTNoC and TISS. The communication is based on a global time (established by a core service, the basic time service). The instant of transmission is known a priori at each participant of communication. Consequently, communication is predictable and deterministic with respect to timing, latency, and arrival time. Furthermore the message order is guaranteed. The global time base is provided by the NoC. Each micro component has a local replication which is synchronized periodically. The NoC is supplied by a reference time through a communication network, such as Time-Triggered Ethernet (TTE).

The fault containment (or encapsulation) is established in two ways. First a micro component is separated from other components via TISS, which ensures fault containment of the micro component (i.e. a fault in the component leads to no violation of the communication specification, the Time-Triggered Schedule). Second each communication channel is encapsulated by the TTNoC, so that other communication channels and the computation of unrelated micro components are not disturbed by a fault in a micro component.

Due to the fact that the core services are deterministic and simple the certification effort is decreased.

2.2 INDEXYS

2.2.1 Overview

The INDEXYS project provides a practical demonstration of the GENESYS design approach on real world embedded systems applications. Using cross domain demonstrators INDEXYS shows how GENESYS approach is not bound to a single industrial domain. There are three use cases from

automotive, aerospace and railway industry, with four different demonstrators. Apart from the research on the impact of GENESYS design approach, INDEXYS also explores the impact of deterministic communication on these use cases and its benefits on different system properties (i.e., reliability, dependability, composability, safety, security etc.). The sensibility of chosen industrial domains, conditioned development of new hardware and software, as well as integration of legacy systems with new technologies based on the GENESYS approach showed to be highly valuable.

2.2.2 Use Case Automotive

As one of the leaders in innovation of safety dependent applications the automotive use case is a perfect match for a testing of the GENESYS approach and an implementation of new mechanisms for deterministic communication. This use case consists out of two demonstrators:

- The CAN Router, and
- The FlexRay MultiRouter.

2.2.2.1 Demonstrator: CAN Router

CAN (Controller Network Area) is an asynchronous fieldbus network used in a wide range of industrial applications. The automotive domain is a frontrunner in usage of CAN networks. CAN networks are simple, decentralized, and low cost which ultimately make it highly acceptable by industrial community. The CAN protocol on the other hand is highly limited when it comes to reliability (e.g., monopolization of bus by a single faulty node).

The CAN router designed and implemented in INDEXYS is based on time triggered paradigm and as a result it increases reliability of a CAN network by a fair margin and overcomes the limitations of the traditional CAN network. It was built using GENESYS principles and it showed benefits of this approach in all stages of development.

The CAN router was implemented on an FPGA platform, with a time-triggered system-on-chip (TTSoC) as a core architectural building block. It extends traditional CAN network such that typically bus structured networks can be transformed into star oriented network with possibility of connecting either individual nodes or complete clusters of nodes. A TTSoC provides temporal fault isolation, which denies a faulty node to disrupt communication of other nodes. In addition it increases a capacity of a network, it provides better diagnostic evaluation capabilities, and it is able to connect legacy CAN devices.

Using deterministic component in a CAN network proved to be highly beneficial for CAN communication networks.

2.2.2.2 Demonstrator: FlaxRay MultiRouter

The second demonstrator investigates FlaxRay multi-routing concept which increases FlexRay capabilities in several aspects. FlexRay is a bus oriented deterministic, fault-tolerant, high-speed communication network. It is created by a consortium gathered around automotive domain. The goal was to create a bus network with high transmission speeds and high reliability constraints. To enforce deterministic behavior FlaxRay uses static configuration. For each change a whole system must be reconfigured. It is a broadcast protocol which doesn't allow parallel multicast or unicast transmissions. This results in inefficient use of bandwidth.

FleyRay MultiRouter provides the possibility of parallel message transmission, by partitioning disjoint communication lines within a single time slot. This means more communication channels on a same number communication slots. It also allows dynamic reconfiguration of channels to some extent.

These options became highly required in automotive industry as a number of ECUs in a car gradually increases with each new generation.

2.2.3 **Use Case Aerospace**

The INDEXYS demonstrators for aerospace investigate applicability of GENESYS architecture in the aerospace domain. It consists of enchantments for Remote Data Concentrator (RDC) and Network Access Controller (NAC).

The RDC component provides an interface between transducers (i.e., sensors and actuators) and the Central Processing Modules, by allowing a standardized network connection to a TTP field bus. Using TTP provides determinism required by the high safety standards in aerospace domain.

It uses a table driven communication layer which solves a problem of emerging certification issues due to rapid increase in size of software modules.

The NAC component controls an access to the backbone network and a central unit (CU) (i.e., server) by a passenger service unit (PSU) in an airplane cabin. It serves as an interface between high speed Ethernet based network (Ethernet, TTEthernet) and up to eight linear buses connected to PSUs.

It provides completely fail safe access with minimal delay in case of single NAC failure. The architecture ensures scalability, reusability, high bandwidths, modularity, fault tolerance and the robustness against transient faults.

2.2.4 **Use Case Railway**

The INDEXYS demonstrator for railway application investigates integration capabilities of the legacy railway systems with the novel time-triggered base communication (e.g., TTEthernet). In the scope of the demonstrator a safety related protocol called One Channel Safe (OCS) developed by Thales is implemented on top of the software based TTEthernet.

The goal of the project was to evaluate usability of GENESYS based services implemented in TTEthernet on a safe communication stack for the railway domain. TTEthernet provides set of services derived from the GENESYS architecture which are highly beneficial for safety related applications with mixed-criticality. The study is compared with rest of the demonstrators presented in the project.

2.3 ACROSS

The ACROSS project develops and implements a cross-domain architecture for embedded Multi-Processor Systems-on-a-Chips (MPSoC) based on GENESYS.

2.3.1 **Overview**

ACROSS targets the development of tailored middleware components and suitable design, development and verification tools to generate a powerful cross-industry platform. Special focus is on certifiability, complexity management, temporal determinism and mixed-criticality integration. Using a MPSoC has several advantages like energy, area efficiency, computational performance and reduction of physical units. But the problems with existing MPSoCs are

- certification due to its complexity,
- temporal determinism – usually MPSoCs contain shared memories and caches which complicate predictability e.g. of worst case execution time and
- error propagation due to unsufficient isolation/independence of the subsystems (which make the certification effort high).

WP 4 T1.1 will base its developments on the GENESYS, INDEXYS and specifically the ACROSS results and will provide a upgraded design of the MPSoC involving more performant CPUs in order to support the use of applications requiring higher computing power than achievable when using the Altera NIOS cores.

2.3.2 Use Case Automotive

The automotive demonstrator consists of automation, control and simulation using the ACROSS MPSoC. In particular the ACROSS MPSoC is used as the control unit of a Hardware in the loop (HiL) test bed for a hybrid vehicle. Each xCU's of the vehicle's hybrid powertrain has been mapped to a core of the MPSoC. Because the control algorithms have already been tested, the main focus lies on MPSoC communication.

The communication between the cores of the MPSoC was realized as virtual CAN to model the test as realistic as possible. Furthermore the control unit was connected to the simulation environment via CAN too. The test bed using the MPSoC has been used for several test stages (from development to test bed) without any modifications, e.g. interfaces to the simulation environment.

The control algorithms had to be executed at 1kHz in hard real-time, accomplished by the real-time operating system PikeOS from SYSGO and AUTOSAR-Personality by OpenSynergy combined with the TTNoC.

2.3.3 Use Case Aerospace

Two aerospace demonstrators using the ACROSS MPSoC have been developed.

2.3.3.1 Demonstrator A

Aerospace demonstrator A was built to evaluate the implementation of several Real-Time Data Distribution Services, e.g. meeting of deadlines, transport priority, destination order, etc., on the ACROSS MPSoC. Furthermore some BEE (a middleware providing services for data sharing and distribution, supporting quality of service concepts) performance parameters have been evaluated too. The test application was a cooperative Unmanned Aerial Vehicle (UAV) system, i.e. several UAVs have to accomplish a specific mission together, testing the interoperability of the ACROSS nodes. Real-time coordination (e.g. adapting swarm behavior to reach the goal or adapting to failures) and sharing of information were the main features of this demonstrator.

The ACROSS platform has been used to run components with different criticality levels, e.g. two components with different criticality levels have been installed on a single core (sharing the same resources). To test platform level diversity a component is installed on another core of the ACROSS platform. Furthermore the ACROSS platform was integrated into a network-centric system including also commercially available platforms. It has been used to show the pros and cons provided when the ACROSS platform is part of a complex system w.r.t. modularity, mixed-criticality integration, certification, etc.

2.3.3.2 Demonstrator B

Aerospace Demonstrator B implements a Degraded Vision Landing Aid (DEVILA) system for helicopters. DEVILA supports pilots with altitude information, when landing in a desert with limited visibility.

Three nodes holding parts of the application are interconnected by the TTNoC. The I/O Gateway Server receives the data from a flight simulator over ARINC 429. The simulator data is forwarded to a processing node calculating the data for the head up display (the altitude information). Finally another node generates the graphical output for the pilot.

The TTNoC ensures high reliability by guaranteed message delivery using a hard real-time schedule. The application of this demonstrator is distributed over several CPUs and the parts with different criticality levels are separated by the TTNoC. This distribution improves performance (the work load is split) and simplifies maintenance, certification and testability (the decomposition simplifies the building blocks of the application.

2.3.4 Use Case Industrial

The focus in the industrial demonstrator was to show the applicability of the ACROSS platform within industrial applications. Hard-real time and interoperability with industrial interfaces (e.g. Profibus) were one of the main goals addressed. For demonstration a part of an existing PLC (Programmable Logic Controller) installation has been replaced by the MPSoC developed within ACROSS.

The IO component was used to bridge the application running on the MPSoC with the rest of the PLC. The application has been copied to three cores to demonstrate Triple Modular Redundancy (TMR). Hence three cores calculate the data for the actuators and send it to the IO component. The IO component votes these messages and transfers it to the PLC connected via Profibus. TMR has been verified with fault injection on the sensor and actuator messages from and to the IO component.

2.4 CRYSTAL

Home-page: www.crystal-artemis.eu/

The ARTEMIS Joint Undertaking project CRYSTAL (CRitical sYSTem engineering AcceLeration) takes up the challenge to establish and push forward an Interoperability Specification (IOS) and a Reference Technology Platform (RTP) as a European standard for safety-critical systems.

This standard will allow loosely coupled tools to share and interlink their data based on standardized and open web technologies that enable common interoperability among various life cycle domains. This reduces the complexity of the entire integration process significantly. Compared to many other research projects, CRYSTAL is strongly industry oriented and will provide ready-to-use integrated tool chains having a mature technology-readiness-level (up to TRL 7).

In order to reach this goal, CRYSTAL is driven by real-world industrial use cases from the automotive, aerospace, rail and health sector and builds on the results of successful predecessor projects like CEASAR, SAFE, iFEST, MBAT on European and national level.

2.4.1.1 Demonstration

Among various results a platform oriented multi core architecture approach is investigated within an automotive demonstration in order validate, verify and test appropriate platform configuration and verification tools developed win the subject part of CRYSTAL.

The results generated by CRYSTAL will support the EMC2 WP 4 T1.1 work by providing inputs to the configuration tools the Task can build on.

2.5 MBAT

Home-page: https://www.mbat-artemis.eu/home/

One of the most important strategic sectors in which Europe is developing, integrating and delivering high-quality products is the transportation domain. Here, high-class safety-related products as e.g. airplanes, cars and trains have a huge market impact. More and more of the market value of these vehicles is gained by embedded systems inside these products, and the number and importance of these embedded systems is steadily growing.

Embedded systems are small & hidden computers (not visible and not directly accessible for end users), often equipped with sensors and actuators which are controlling (parts of) the overall system (or product) in which they are embedded. Examples of embedded systems in transportation products are motor controllers, auto pilots, anti-lock braking systems, electronic stability controllers and lane assisting control systems. These type of systems are sometimes also called embedded intelligent systems as they are providing a virtual kind of intelligence to the product containing the embedded systems for the end user of the product (e.g. for a driver or a passenger).

One of the most important enablers to assure the quality of embedded systems is the application of powerful validation and verification (V&V) technologies accompanying the embedded systems development process. Unfortunately, the V&V technologies already in industrial use are still too expensive while often not effective enough.

ARTEMIS project MBAT will provide European industry with a new leading-edge V&V technology in form of a Reference Technology Platform (MBAT RTP) that will enable the production of high-quality and safe embedded systems at reduced cost in terms of time and money. This will be made possible by a new and very promising approach in which model-based testing technologies will be combined with static analysis techniques. Besides this combination, a further new approach is to use (and re-use) specially designed test & analysis models as basis for model-based V&V. This advanced model-based V&V technology will lead to a more effective and at the same time cost-reducing approach compared to traditional ones. In addition, MBAT RTP will be connected to other ARTEMIS RTPs to extend existing platforms. Developed by industrial key players (large companies and SMEs) in this domain and supported by leading research partners, the MBAT RTP will be of high value for the European industry, providing very effective means to assure utmost quality embedded systems at reduced costs.

MBAT results will be used in order to conduct more efficient V&V work in EMC^2 WP 1 T1.1 achievements.

2.6 RECOMP

Home-page: http://atcproyectos.ugr.es/recomp/

The RECOMP research project undertakes to form a joint European task force contributing to the European Standard Reference Technology Platform for enabling cost-efficient certification and re-

certification of safety-critical systems and mixed-criticality systems, i.e. systems containing safety-critical and non-safety-critical components. The aim is establish methods, tools and platforms for enabling cost-efficient (re-)certification of safety-critical and mixed-criticality systems. Applications addressed are automotive, aerospace, industrial control systems, lifts and transportation systems.

RECOMP recognizes the fact that the increasing processing power of embedded systems is mainly provided by increasing the number of processing cores. The increased numbers of cores is a design challenge in the safety-critical area, as there are no established approaches to achieve certification. At the same time there is an increased need for flexibility in the products in the safety-critical market. This need for flexibility puts new requirements on the customization and the upgradability of both the non-safety-critical and safety-critical parts. The difficulty with this is the large cost in both effort and money of the re-certification of the modified software.

RECOMP will provide reference designs and platform architectures, together with the required design methods and tools, for achieving cost-effective certification and re-certification of mixed-criticality, component based, multicore systems. The aim of RECOMP is to define a European standard reference technology, supported by the European tool vendors participating in RECOMP (see Figure 2).

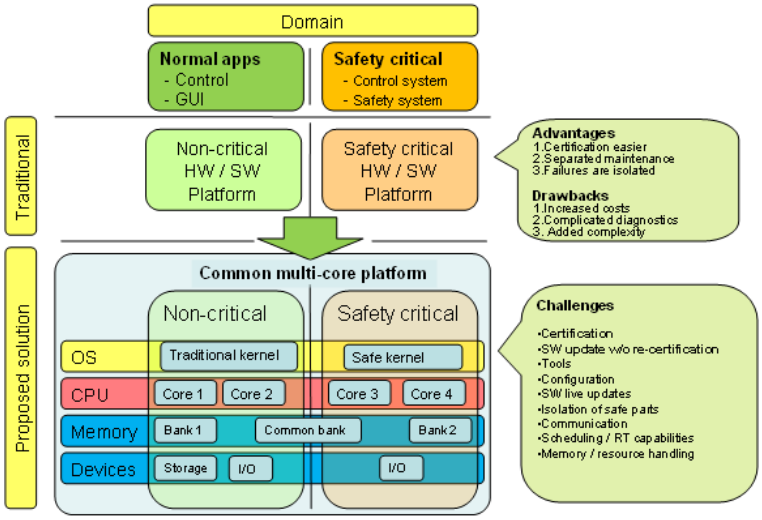

Figure 2: RECOMP Approach

EMC² WP 1 T1.1 will on top of using the ACROSS MPSoC results also investigate the RECOMP achievements in order to incorporate the best of all approaches stemming from European project results.

2.7 SMECY

Multi-core technologies are strategic to keep and win market shares in all areas of embedded systems. SMECY's mission is to develop new programming technologies enabling the exploitation of these multicore architectures.

Multi core programming cannot be managed in a "by hand" approach. The variability of cores requires correction by software. The designer needs ways to express /extract / exploit parallelism depending on both, platform and application.

Since it is now feasible to integrate more than a billion transistors on a single silicon chip, the number of processor cores per chip will rise above one hundred in the next couple of years. As the number of cores increase, traditional multiprocessor techniques will no longer be efficient and this will require new approaches. However, the grand challenge is how to program these parallel platforms to fully exploit the available computing power efficiently within reasonable efforts. In the short term, an even more urgent

challenge is how to transform current non-scalable, sequential, legacy assets to run on multi-core platforms.

The vision of the SMECY consortium is a holistic approach for the integration of multi-core SOC and embedded software technologies. To find such an approach, interactive research and development of programming and design methods, multi-core architectural solutions and associated supporting tools are needed. All of this is strongly driven by the requirements and constraints from different application areas as well as the target platform. The conceptual approach of the SMECY project is depicted in Figure 3. The front end/back end takes both, the application requirements and the platform constraints into account to become efficient.

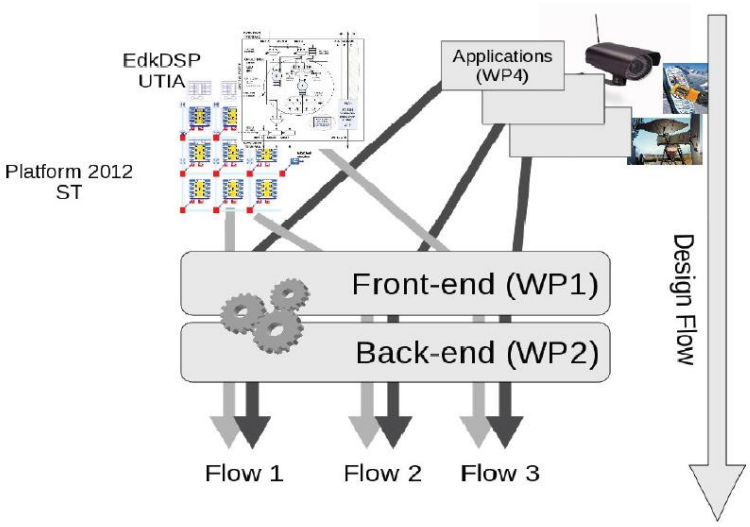

Figure 3: SMECY Approach

Concerning the EMC² WP 1 T1.1. work the considerations of SMECY will be respected. The useful output of the project will be carried on in order to generate a multi-core oriented solution for EMC² with best efficiency and performance.[1]

2.8 ENTRA

Homepage: http://entraproject.eu/

ENTRA is a 3-year research project funded by the EU 7th Framework Programme Future and Emerging Technologies (FET). The project runs from the 1st October 2012 to the 30th September 2015 and aims to promote "energy-aware" software development using advanced program analysis and modelling of energy consumption in computer systems. The project will facilitate predictions of energy consumption to be made early in the software design phase, thus enabling the development of greener IT products.

EMC² WP 1 will contact the ENTRA project and will investigate to join forces for cooperation.

2.9 FLEXTILES

Homepage: www.flextiles.eu/

[1] The information is taken from the ARTEMIS JU Project flyer for SMECY.

A major challenge in computing is to leverage multi-core technology to develop energy-efficient high performance systems[2]. This is critical for embedded systems with a very limited energy budget as well as for supercomputers in terms of sustainability. Moreover the efficient programming of multi-core architectures, as we move towards many-cores with more than a thousand cores predicted by 2020, remains an unresolved issue. The FlexTiles project will define and develop an energy-efficient yet programmable heterogeneous many-core platform with self-adaptive capabilities.

The manycore will be associated with an innovative virtualisation layer and a dedicated tool-flow to improve programming efficiency, reduce the impact on time to market and reduce the development cost by 20 to 50%.

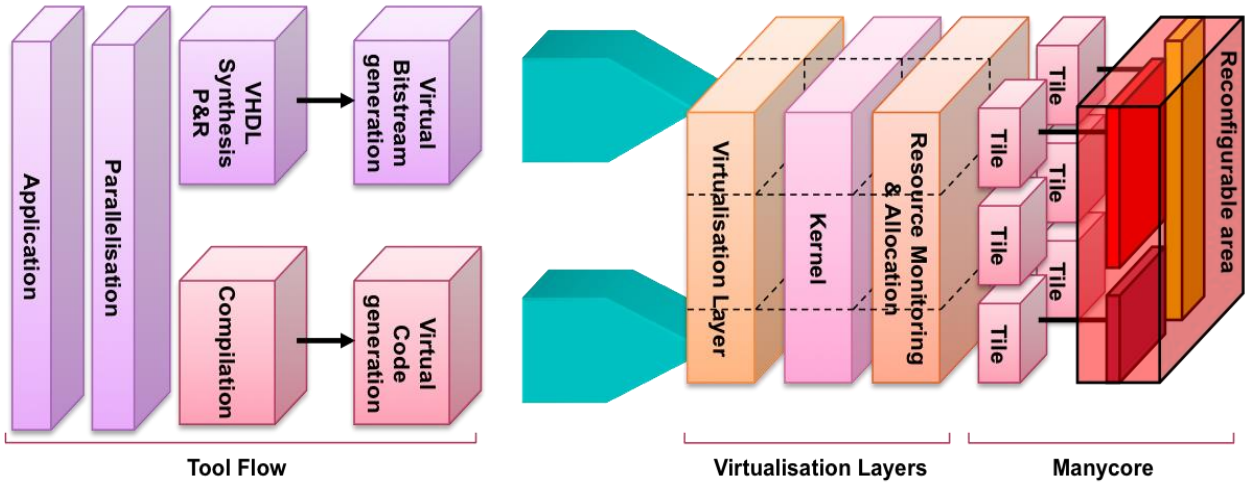

Figure 4: FlexTiles approach

FlexTiles will raise the accessibility of the many-core technology to industry – from small SMEs to large companies – thanks to its programming efficiency and its ability to adapt to the targeted domain using embedded reconfigurable technologies.

FlexTiles is a 3D stacked chip with a many-core layer and a reconfigurable layer. This heterogeneity brings a high level of flexibility in adapting the architecture to the targeted application domain for performance and energy efficiency.

A virtualization layer on top of a kernel hides the heterogeneity and the complexity of the many-core and fine-tunes the mapping of an application at runtime. The virtualization layer provides self-adaptation capabilities by dynamically relocation of application tasks to software on the many-core or to hardware on the reconfigurable area. This self-adaptation is used to optimize load balancing, power consumption, hot spots and resilience to faulty modules.

The reconfigurable technology is based on a virtual bit-stream that allows dynamic relocation of accelerators just as software based on virtual binary code allows task relocation. This flexibility allows the use of fault mitigation schemes, a crucial issue for future many-cores. During the execution of the application, the runtime binding is done to match the configuration defined by the virtualization layer. It adapts the location of the code, the storage and the communication paths on the fly.

Contacts will be established via partners in the project that are members of the FlexTiles consortium in order to benefit from the achievements in FlexTiles in particular in the area of dynamic reconfiguration.

[2] The information is taken from: http://flextiles.eu/WordPress3/

2.10 DeSyRe

Homepage: www.desyre.eu/

The DeSyRe project performs research on the design of future reliable Systems-on-Chip (SoCs). These are systems that guarantee continuous and correct operation in the existence of different types of faults. It is a well-known fact that various systems are extremely sensitive to faults; typical examples are medical embedded systems, in which a single malfunction will put the life of a patient in danger.

However, as semiconductor technology scales, chips are becoming ever less reliable; prominent reasons for this phenomenon are the sheer number of transistors on a given silicon area and their shrinking device features. As a consequence, fault tolerance, provided through various redundancy schemes, comes at an enormous increase in power cost and performance overheads. To make matters worse, power-density is becoming a significant limiting factor for performance and SoC design in general. In the face of such changes in the technological landscape, current solutions for fault-tolerance are expected to introduce an excessive overhead in future SoCs.

At the increasing fault-rates, expected in the upcoming technology generations, DeSyRe will develop new design techniques for future SoCs, improving their reliability and reducing their power and performance overheads for fault-tolerance.

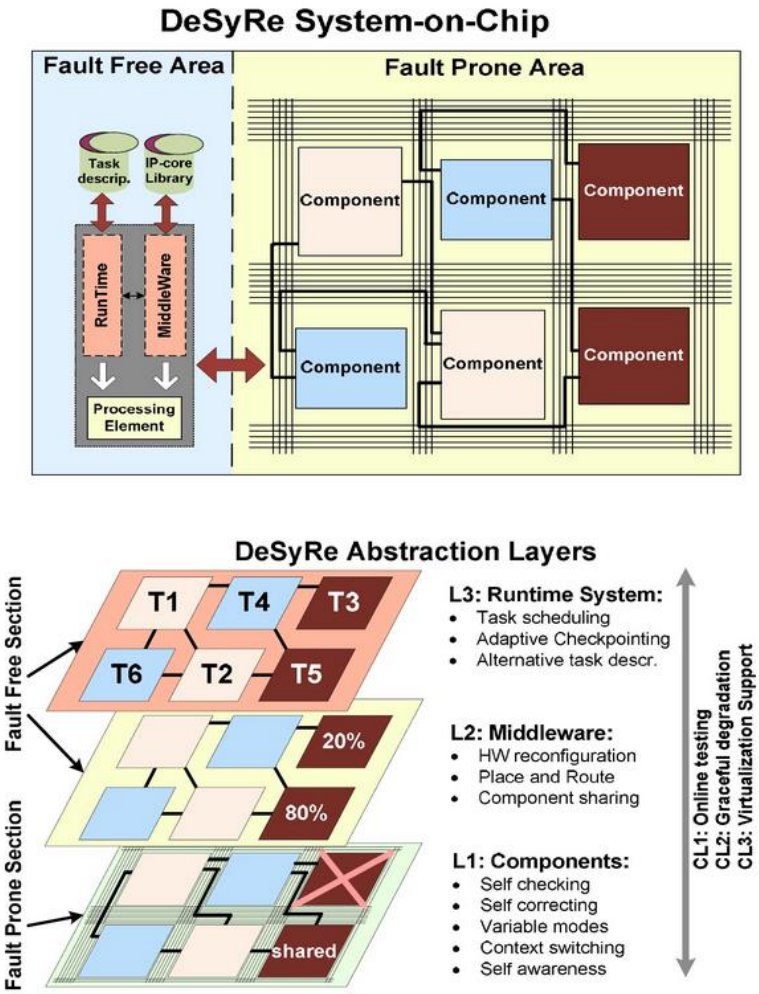

Figure 5: DeSyRe approach

Designing and manufacturing totally fault-free systems has a heavy even prohibitive impact in its cost and performance. Instead, in DeSyRe we will design fault-tolerant systems built out of unreliable components, rather than aiming at totally fault-free chips. Only a small fraction of a DeSyRe chip will be required to be fault-free; this fraction will then be assigned the critical task of monitoring and maintaining the correct operation of the remaining unreliable (fault-prone) chip-resources which are responsible for the main functionality of the SoC.

In addition, DeSyRe SoCs will be on-demand adaptive to various types and densities of faults, as well as to other system constraints and application requirements. For leveraging on-demand adaptation/customization and reliability at reduced cost, DeSyRe will employ three abstraction layers: the Runtime System and Middleware software layers, running on the fault-free part of the SoC, and the Components layer, composing the fault-prone area of the chip. The DeSyRe Components will deliver the functionality of the targeted SoC and will be built on a new dynamically reconfigurable substrate to provide flexibility and adaptation. The Middleware layer will be responsible for the dynamic reconfiguration of the fault-prone (reconfigurable) area in order to adapt the system, isolate and correct faults. Finally, the Runtime System layer has the top-level overview of the system; it manages the on-chip resources based on the application requirements (e.g. performance, functionality) and the system constraints (e.g., available resources, types and densities of faults).

EMC^2 will establish contact and is in particular interested in the increased fault-tolerance findings and innovations made as well as in the how to increase chip reliability.

2.11 MERASA/parMERASA

Homepages: http://ginkgo.informatik.uni-augsburg.de/merasa-web/ and http://www.parmerasa.eu/

Providing higher performance than what state-of-the-art embedded processors can deliver today will increase safety, comfort, number and quality of services, lower emissions and fuel demands of automotive, aerospace, space, and construction machinery applications. Multi-core processors are increasingly being considered as the solution to achieve an increased processor performance, while maintaining low chip costs and low power consumption. However, current trends in mainstream multi-core processor design result in processors with certainly reduced average execution times, but typically with unpredictable and un-analyzable (or extremely pessimistic) worst case behavior that deems them unusable in the domain of safety-related real-time embedded systems.

The MERASA project will develop multi-core processor designs (from 2 to 16 cores) for hard real-time embedded systems hand in hand with timing analysis techniques and tools to guarantee the analyzability and predictability regarding timing of every single feature provided by the processor. Design exploration activities will be performed in conjunction with the timing analysis tools. The project will address both static WCET analysis tools (the OTAWA toolset) as well as hybrid measurement-based tools (RapiTime) and their interoperability. It will also develop system-level software with predictable timing performance.

To constrain production costs and technology integration risks, we investigate hardware-based real-time scheduling solutions that empower the same multi-core processor to handle hard, soft, and non-real-time tasks on different cores. The developed hardware/software techniques will be evaluated by application studies from aerospace, automotive, and construction-machinery areas performed by selected industrial partners.

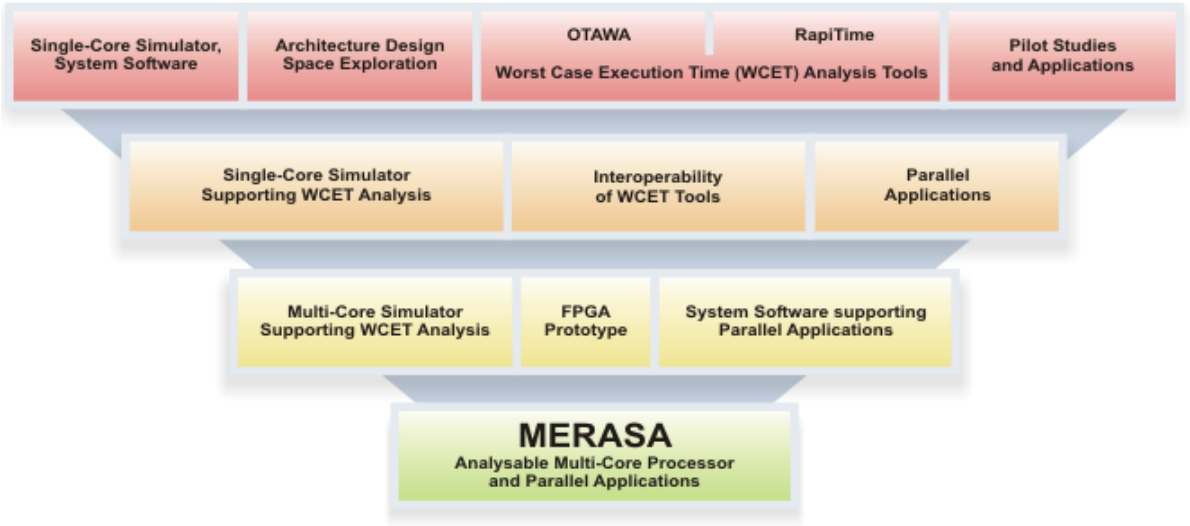

Figure 6: MERASA approach

EMC² WP 1 T1.1 is especially interested in the approach to increase performance and to investigate how to implement parallel processing approaches in order to optimize the designs planned.

2.12 SCALOPES

The project focuses on cross-domain technology and tool developments for *multi-core architectures* (http://www.artemis-ia.eu/project/7-scalopes.html). These developments will be driven by and proven for 4 different application domains. Focus in the technology developments will be on application & programming models, composability, dependability, reliability, predictable system design, resource management and tools supporting these new developments.

EMC² is interested in the tools approach of the SCALOPES project.

3. Conclusions

In the previous chapters we summarized industrial demonstrators and achievements from the several projects, in particular GENESYS, INDEXYS and ACROSS, financed by European Union and Joint Undertaking initiatives, member states and individual member partners in quite some detail. All three projects were completed successfully and provided excellent results. The projects were driven by an idea of service oriented architecture (SoA), which could be applied independent of a hardware platform or an industrial domain.

SoA devised in GENESYS is an approach which defines three different sets of services: basic, optional and domain specific. It allows systems from different domains to share basic properties by design, and still be able to integrate specific functions reserved for that domain only. This approach increases the development rate of a system and significantly reduces costs.

The projects ACROSS and INDEXYS used this method to develop fully functional industrial prototypes. The success of the demonstrators also proved how effective the SoA approach can be and that it is certainly a valid way for the future of developing cyber-physical systems.

In addition to these projects that are seen as the basis of the WP 1 T1.1 work, several other EC funded projects provided significant results that will contribute to optimize the design and development work in EMC^2.

4. References

[1] EMC2 High Level requirements document

[2] Kopetz, H., The Complexity Challenge in Embedded System Design, in Proc. of ISORC, May 2008, IEEE Press, pp.3-12, May 2008

5. Appendix

5.1 Abbreviations

Table 1: Abbreviations

Abbreviation	Meaning
EMC²	Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments
µC	Micro-Controller
TISS	Trusted Interface Subsystem
TTNoC	Time-Triggered Network-on-Chip

5.2 Title of appendix section

WP 4 T4.1 Requirements EXCEL List (File name: Requirements_Document_D0401_V06.xlsx)