Xilinx SDSoC for Acceleration of Real-time Video Processing on 'COTS' ZYNQ Modules.

HiPEAC EMC2 Workshop – 2016-01-20

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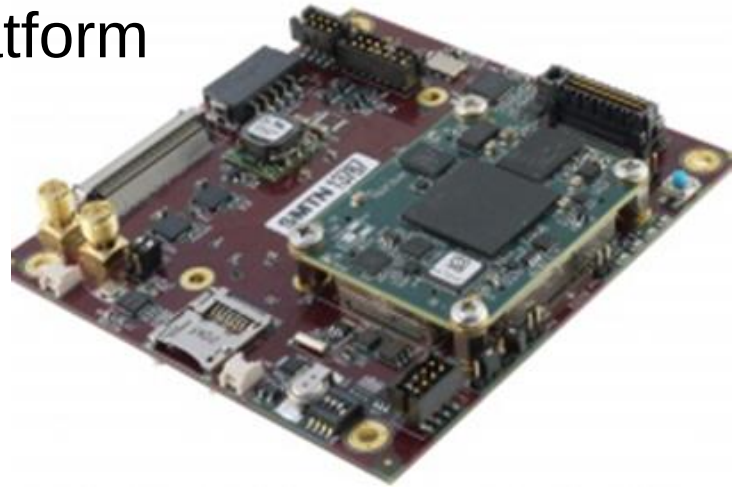
Introduction and Content

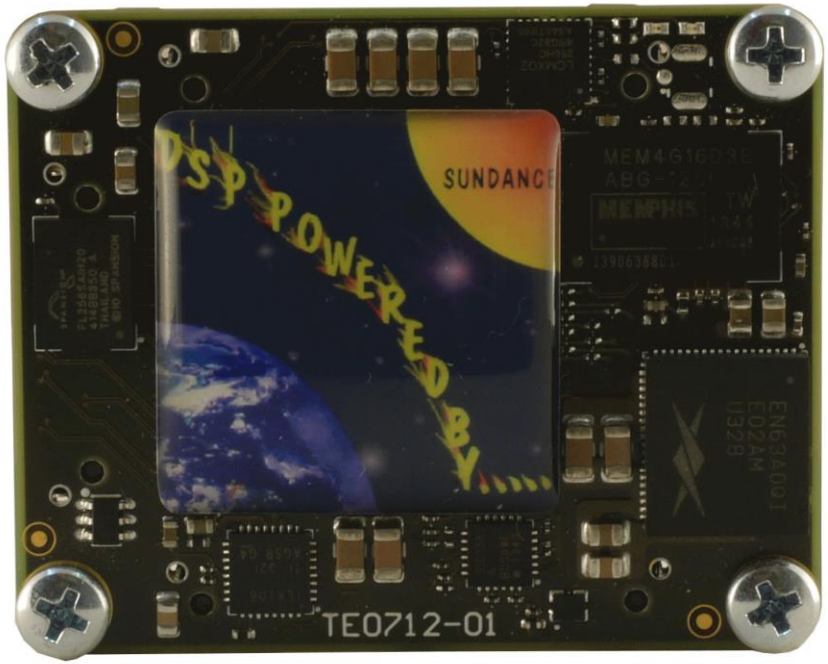
- Introduction to the Xilinx SDSoC Environment

- UTIA SDSoC 2015.4 HW Platform for **EMC²**-DP
  - HDMI-in – HDMI-out Demos
  - VITA Video Sensor-in HDMI-out Demos,
  - Data movers and HLS blocks

- Sundance's **EMC²** Development Platform

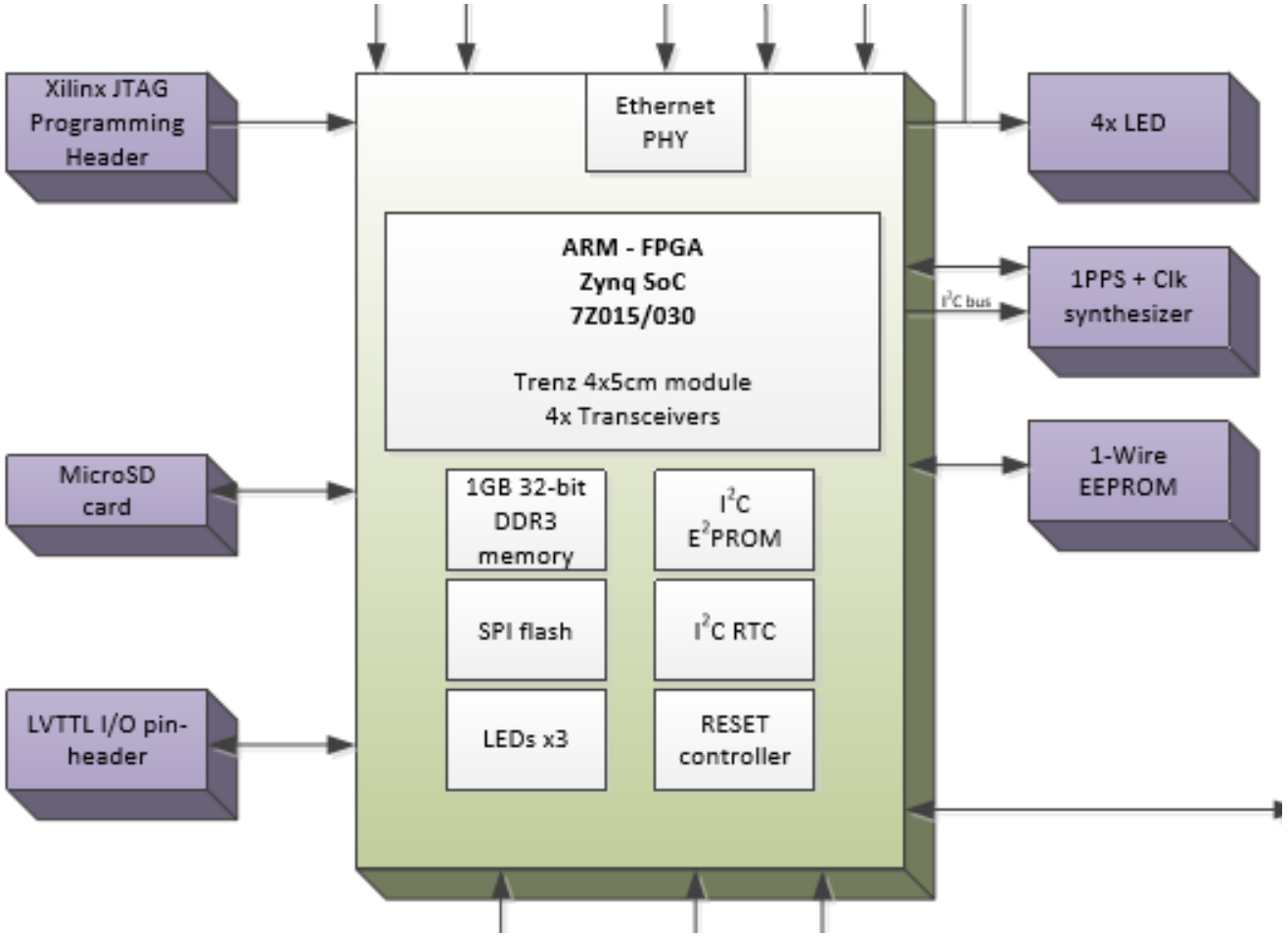


EMC² - System on Module

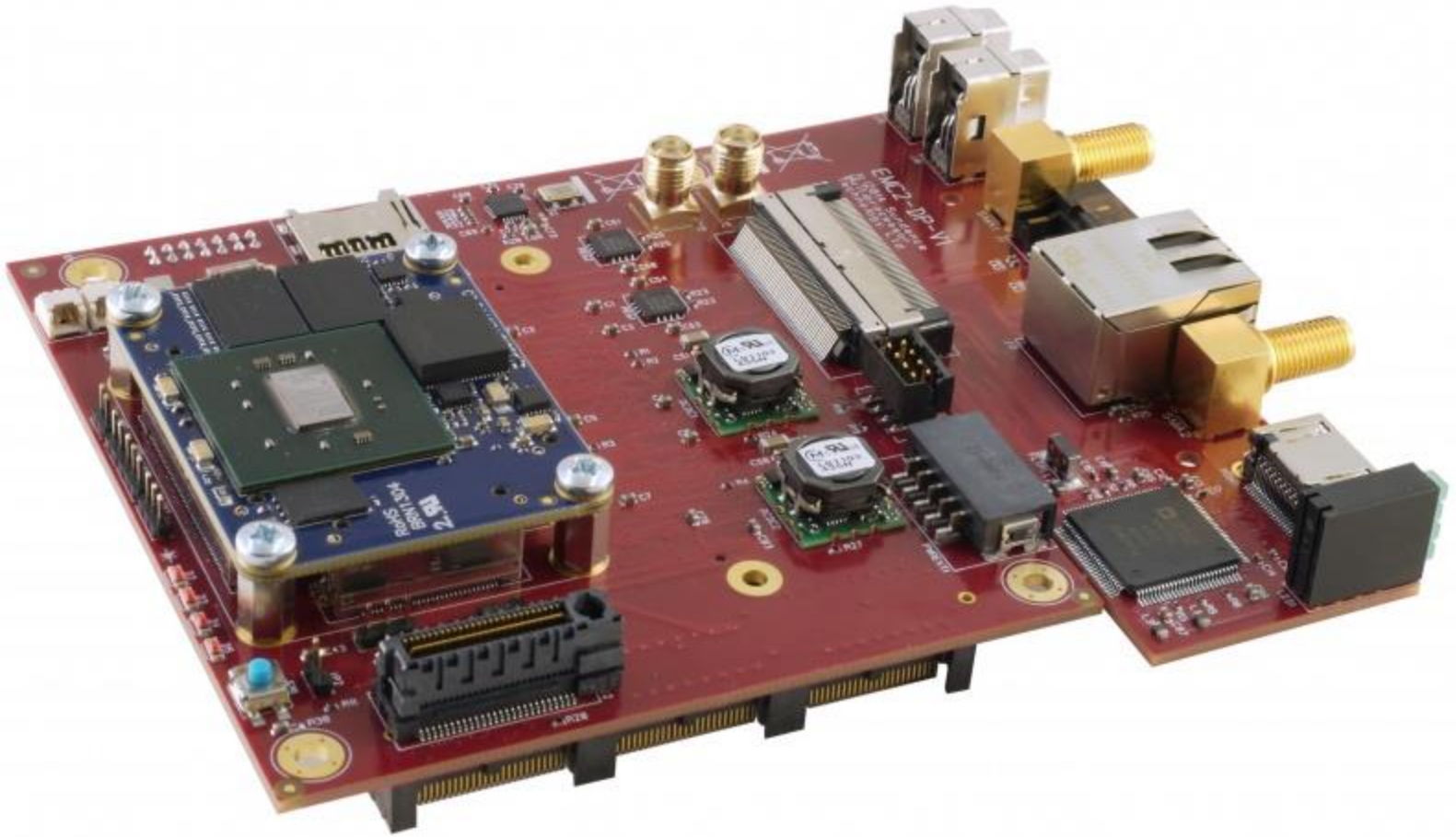


40mm x 50mm
Xilinx SoC or FPGAs
Zynq, Artix-7 or Kintex-7

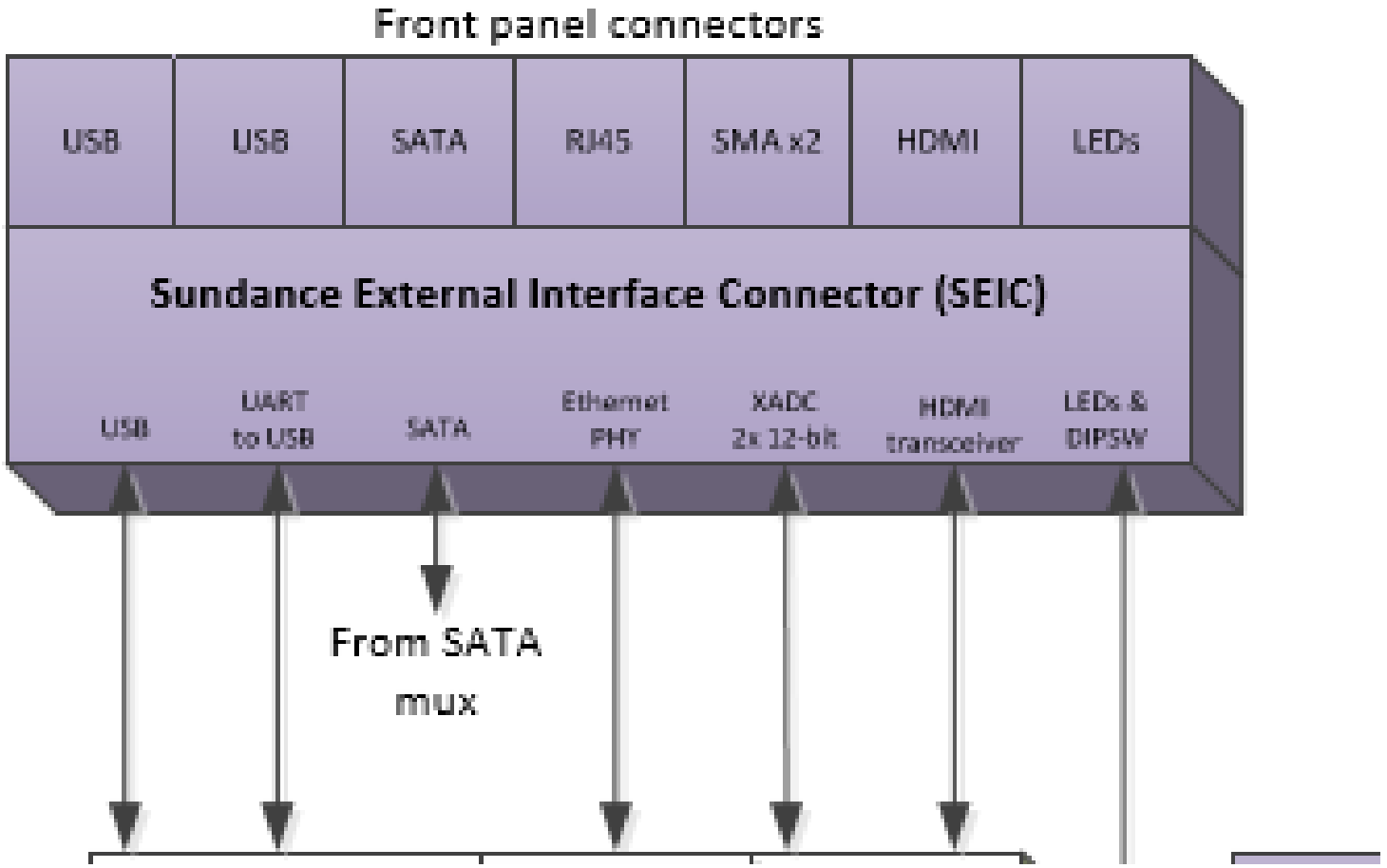
EMC² - System on Module



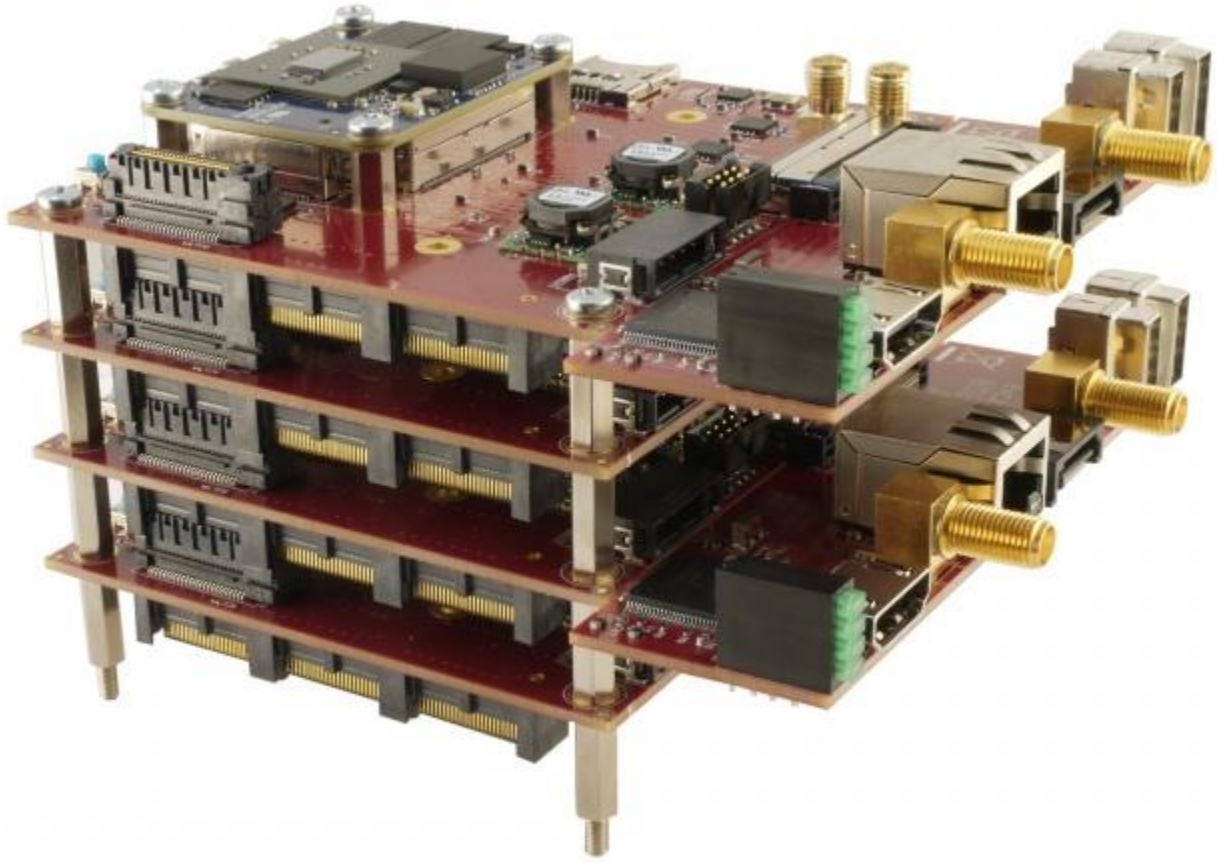
EMC² - Devlopment Platform ‚PC/104 Stackable Board‘



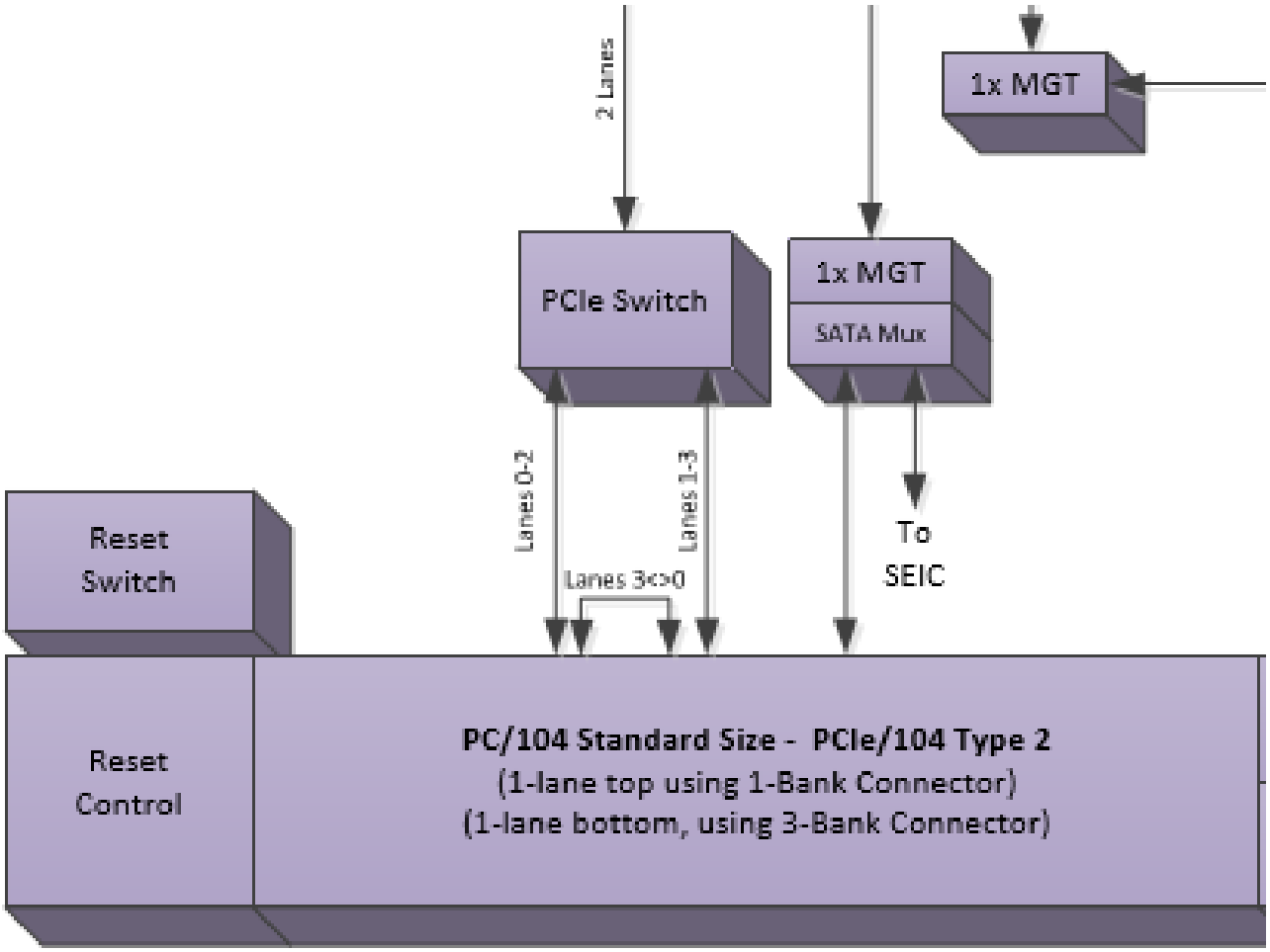
EMC² - Development Platform ‚PC/104 Stackable Board' - IO Module



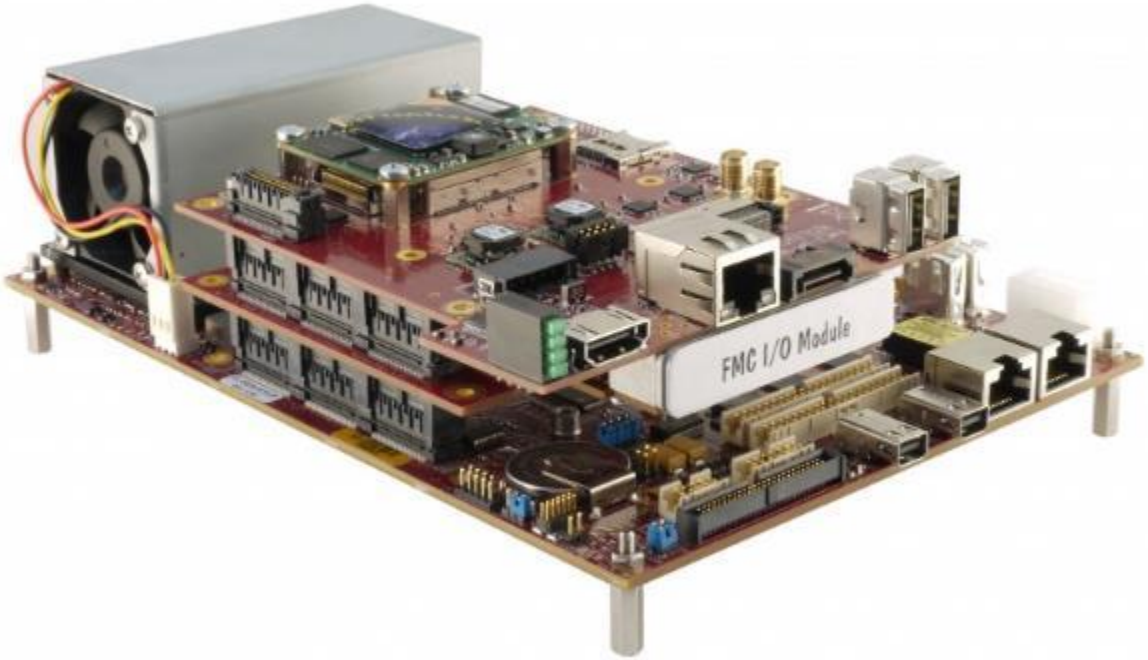
EMC² – Development Platform ‚PC/104 Multiprocessing Stack'



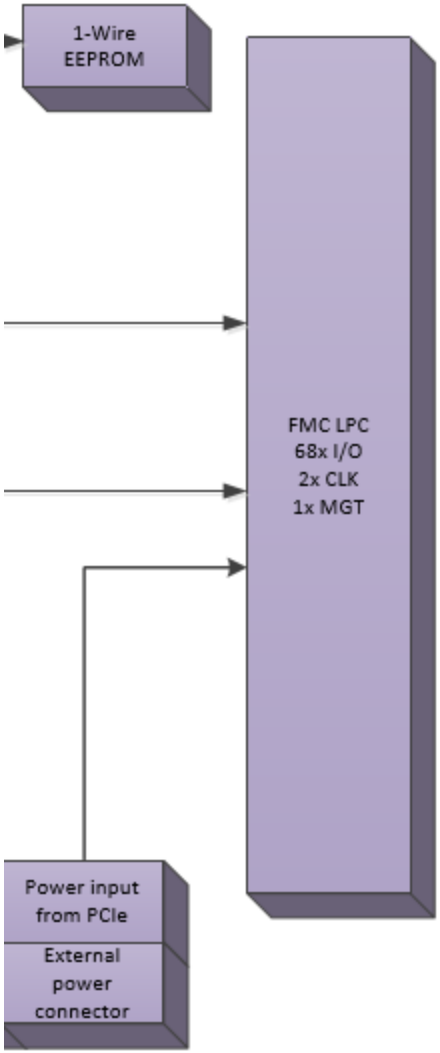
EMC² - Development Platform ‚PC/104 Multiprocessing Stack'



EMC² - Development Platform ‚PC/104 I/O FMC Expansion Module‘

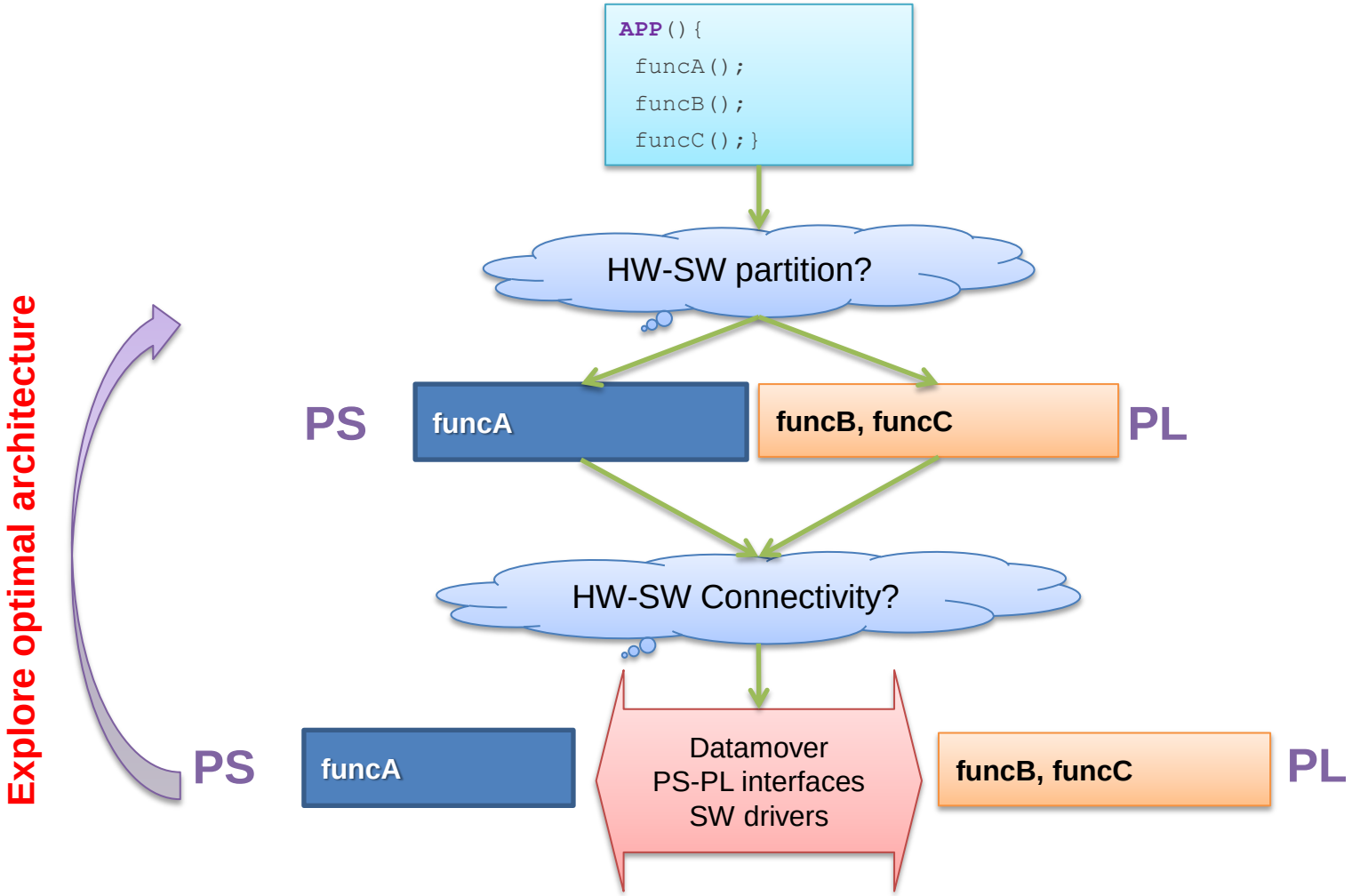


EMC² - Development Platform ‚PC/104 I/O FMC Expansion Module‘

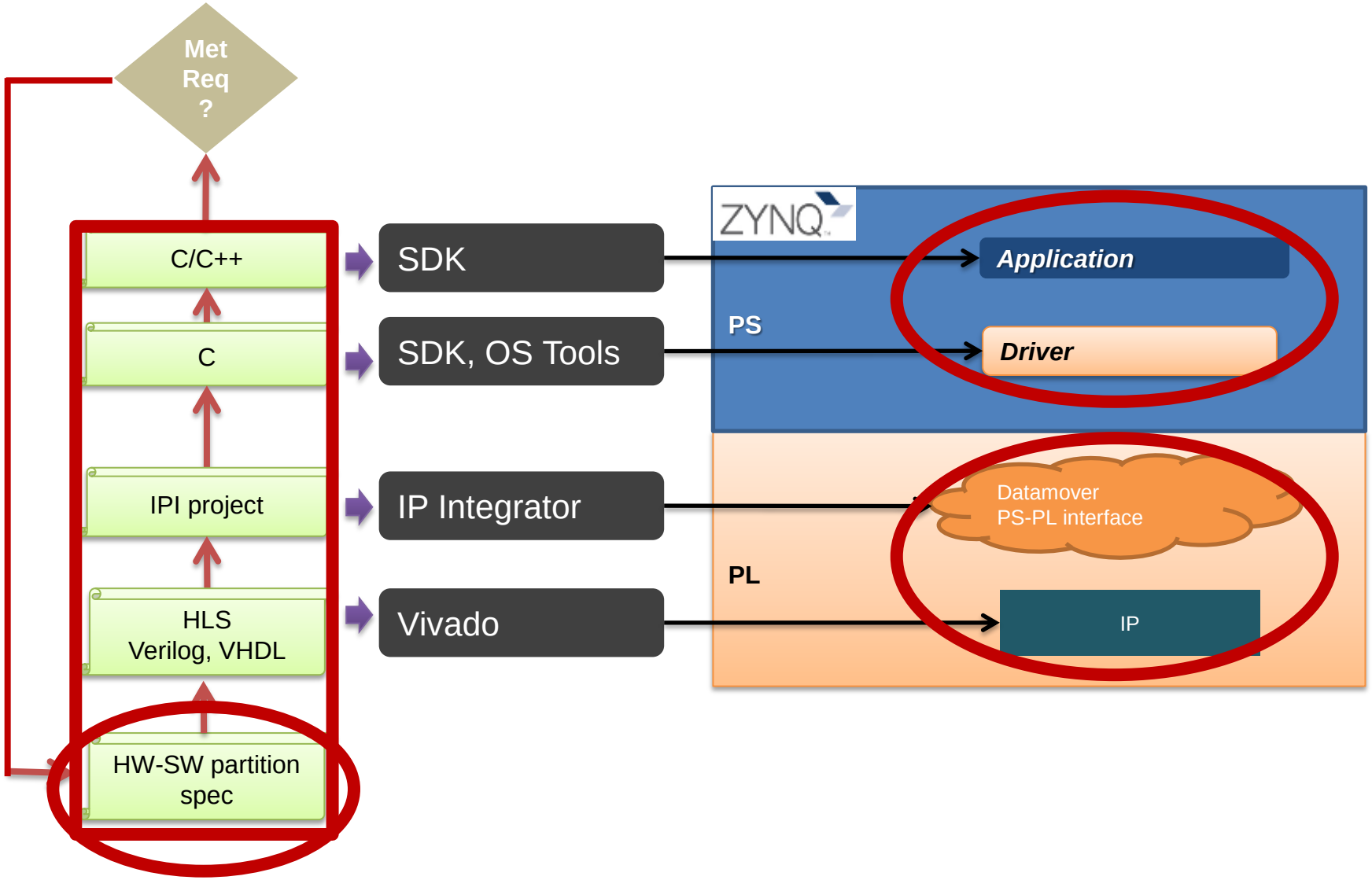


EMC² Video Processing Demo
Xilinx SDSoC Environment

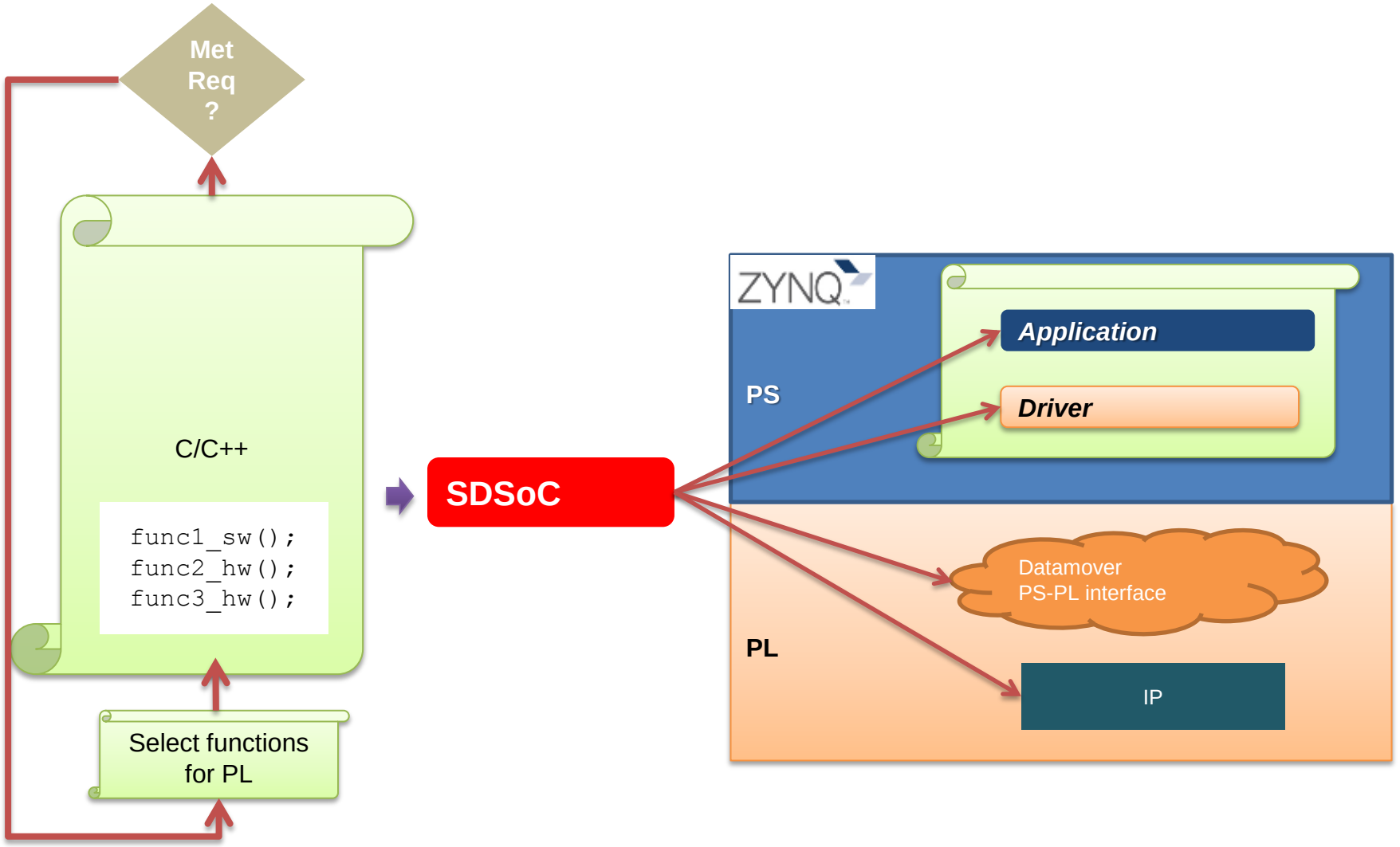
All Programmable SoCs Development Flow



Without SDSoC: HW-SW Partition Exploration

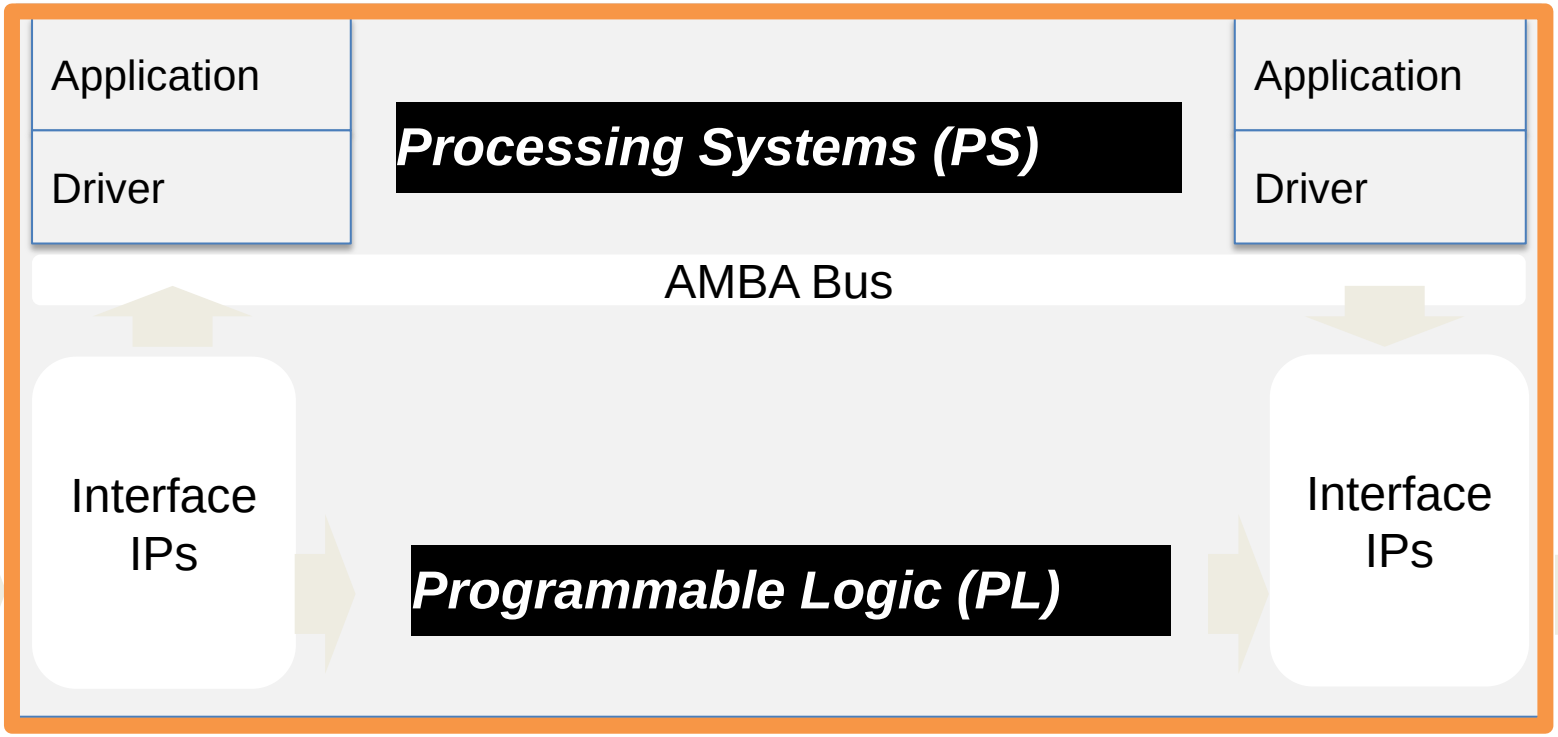


With SDSoC: Automatic System Generation



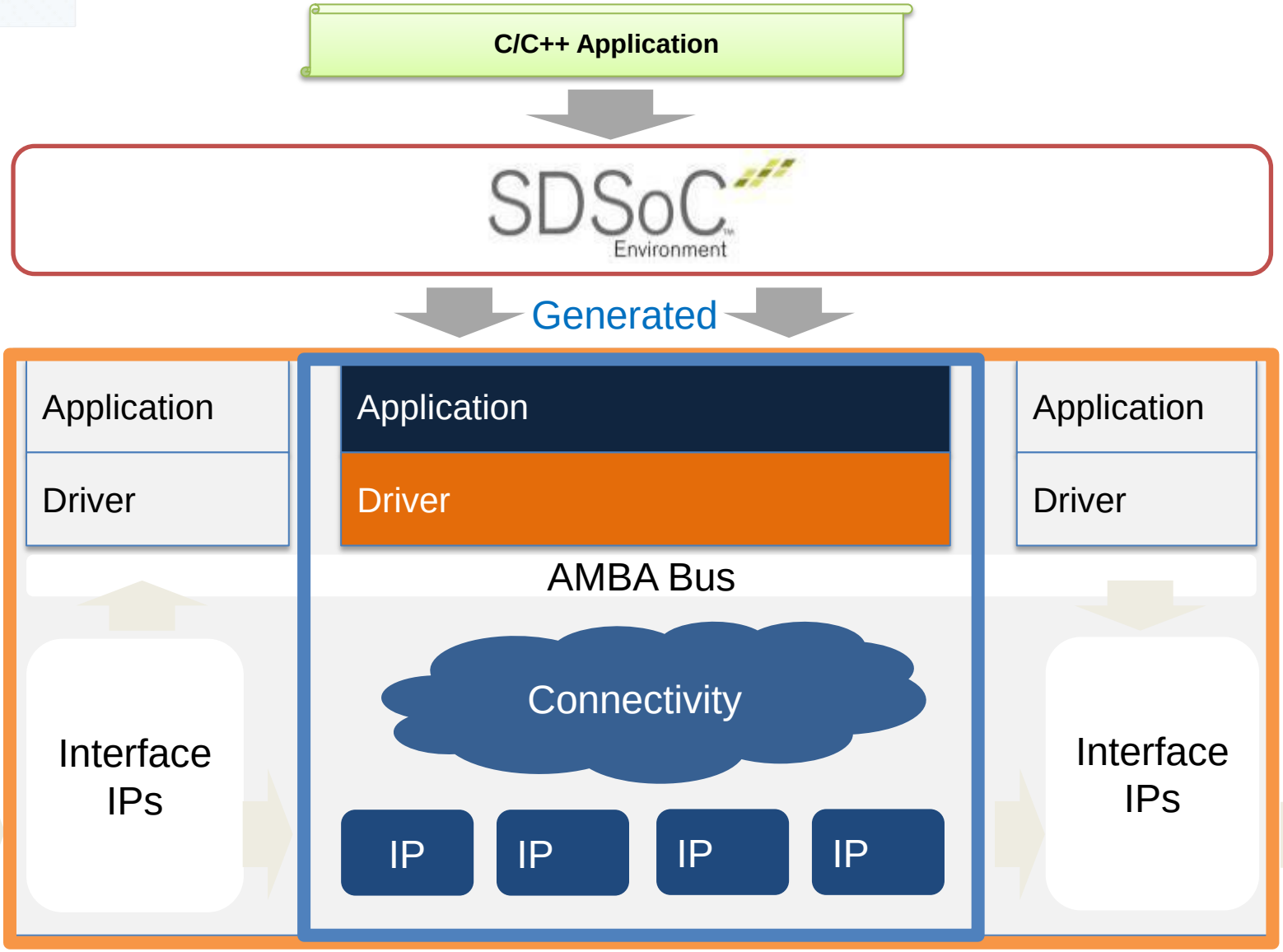
Base HW Platform for SDSoC

- Custom platform = Vivado project + Bootable software image
- Available for commonly used development kit and SoMs



Platform

Complete SDSoC flow



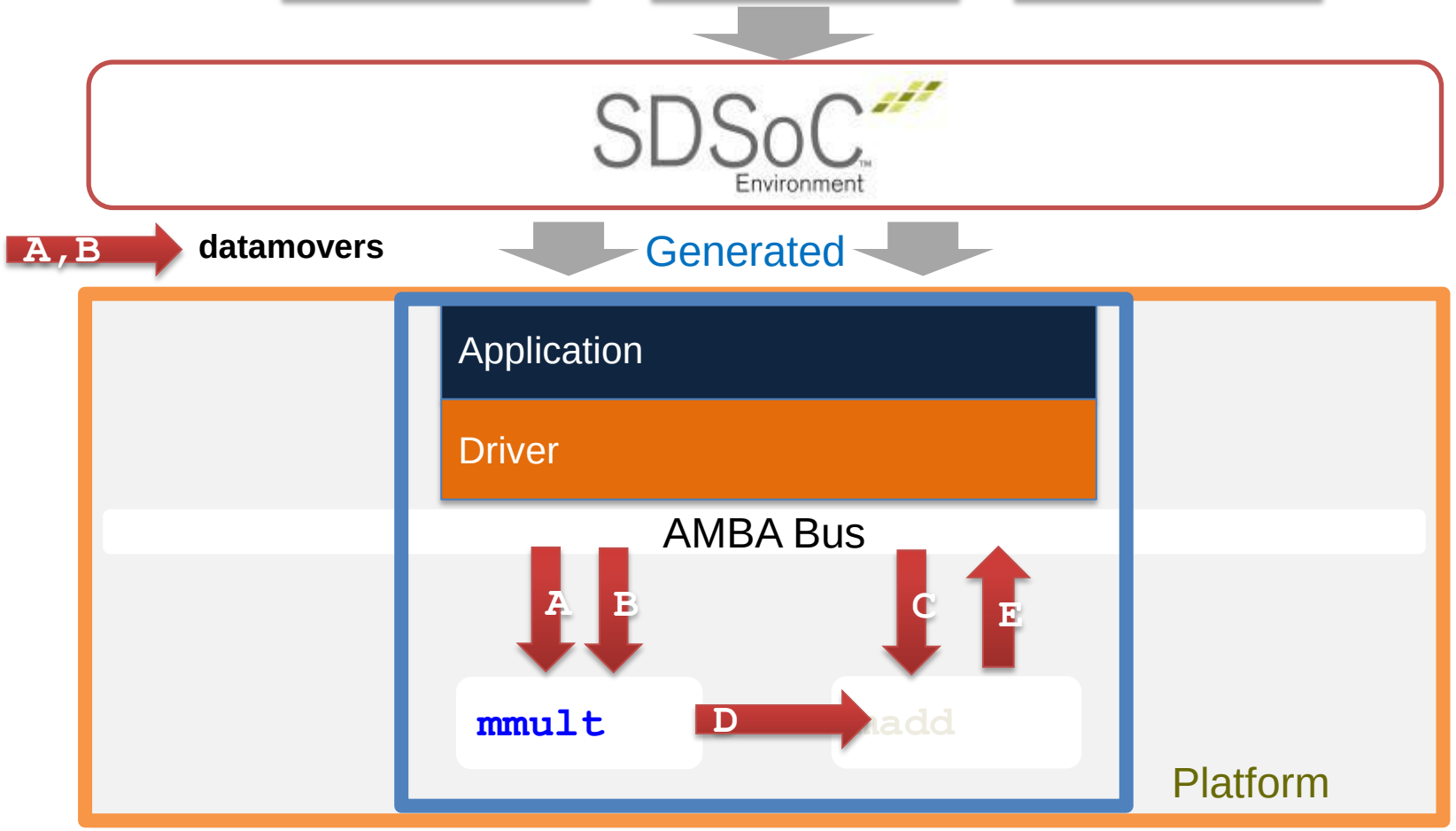
SDSoC Example: Matrix Multiply +Add

C-callable IP

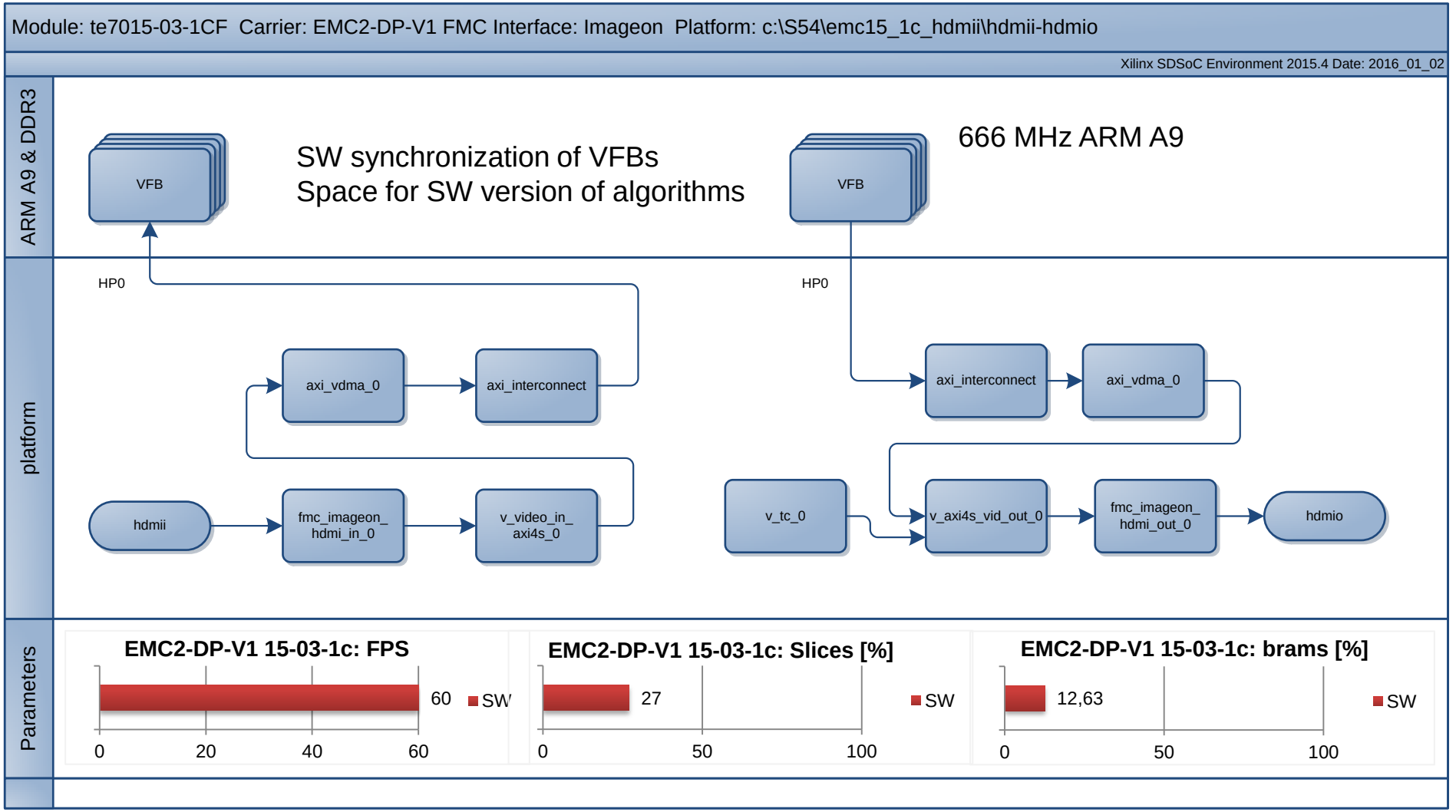
```
madd(inA,inB,out){
  HDL IP
}
```

```
main(){
  malloc(A,B,C);
  mmult(A,B,D);
  madd(C,D,E);
  printf(E);
}
```

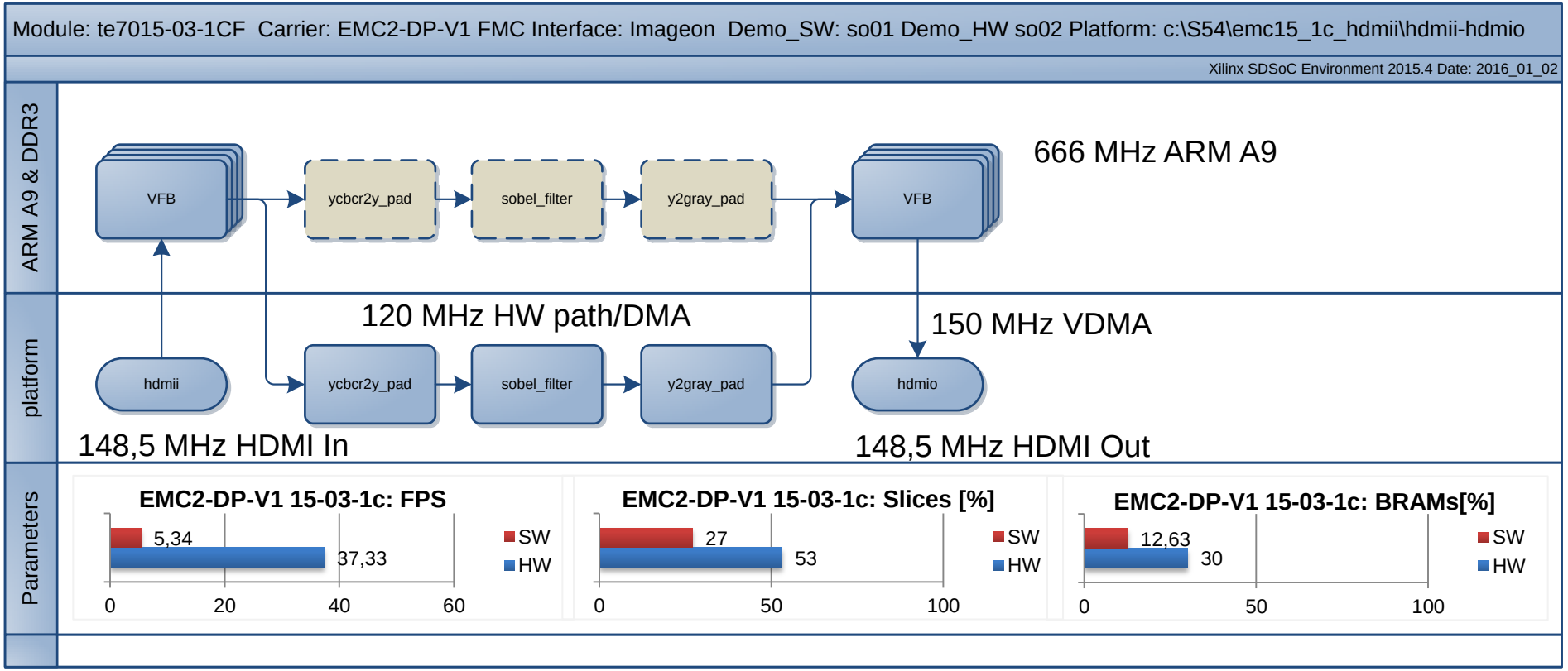
```
mmult(inA,inB,out){
  HLS C/C++
}
```



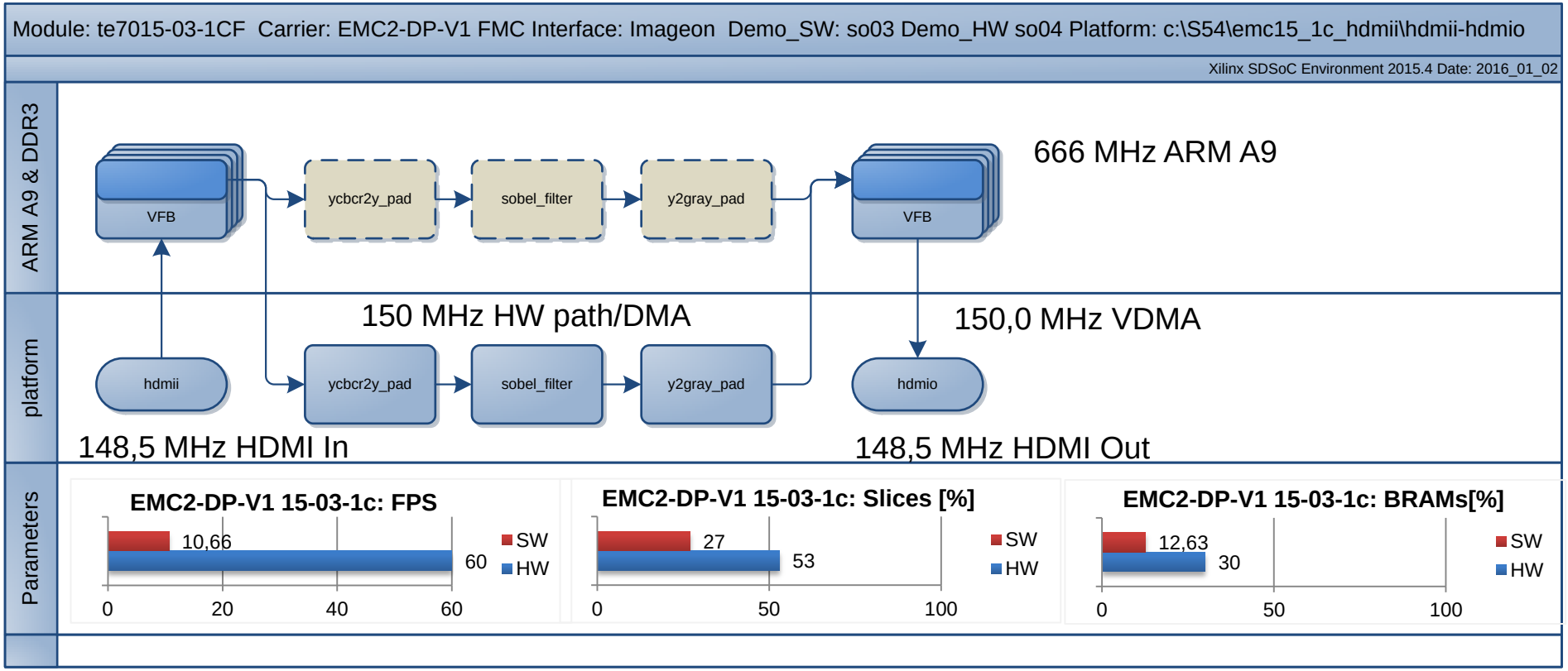
EMC² – DP w. HDMI In/Out FMC Module runnung SDSoC 2015.4 environment



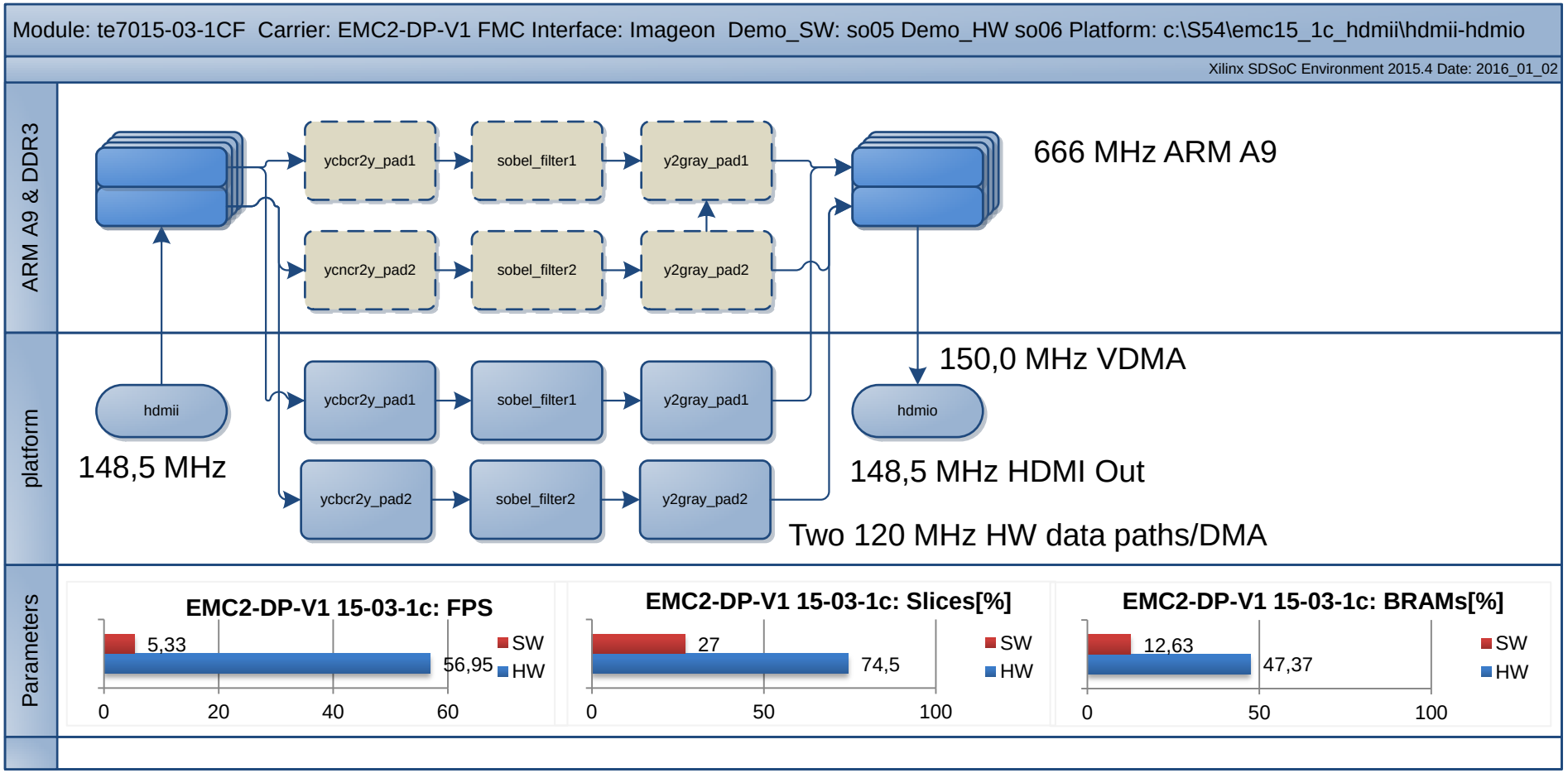
Sobel Filter Full HD Pf: HDMI In/Out SW and HW flow in Xilinx SDSoC 2015.4 Carrier: EMC2-DP



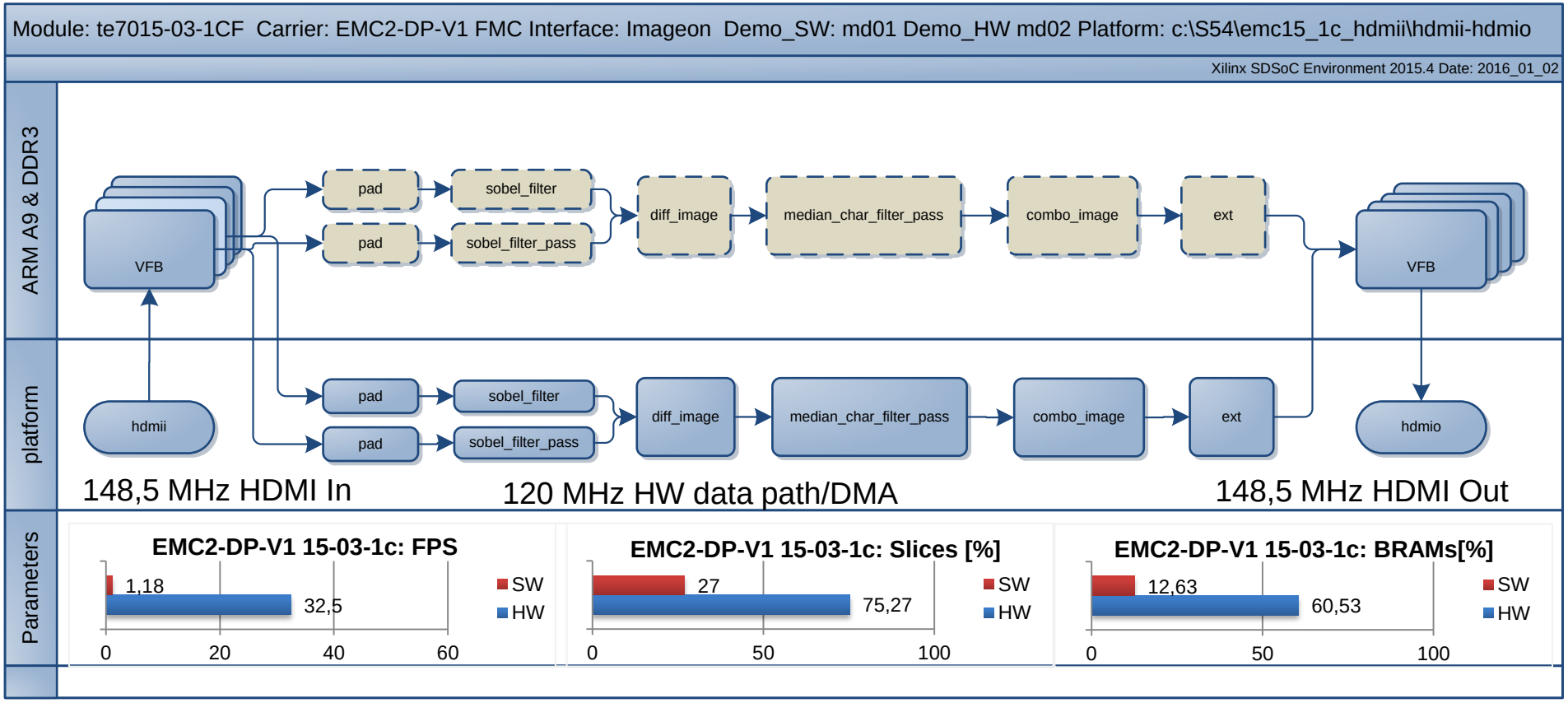
Sobel Filter Full HD Pf: HDMI In/Out
Process only upper 50% of frames
Single computing data path in HW



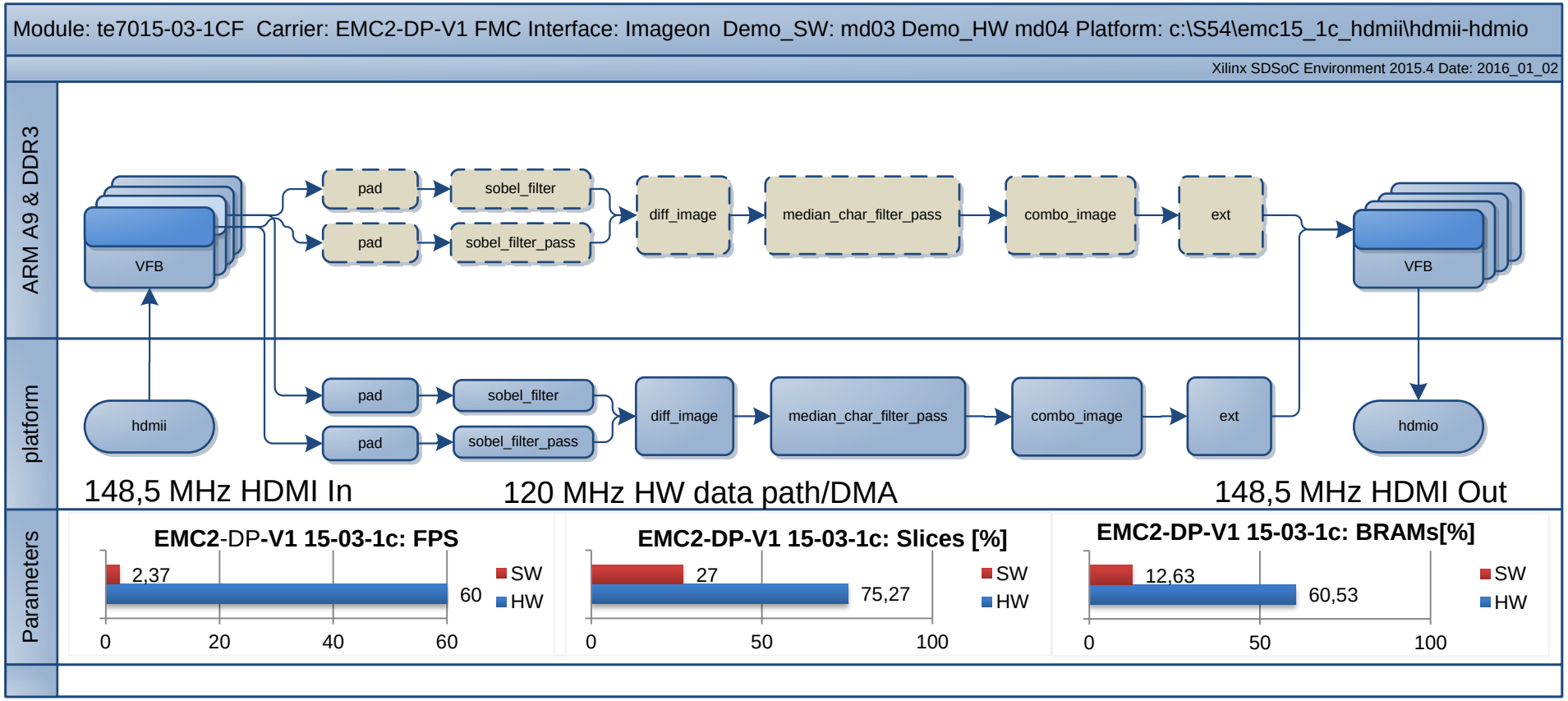
Sobel filter in Full HD Pf: HDMI In/Out
Process upper and lower part of frames
Two parallel computing data paths in HW



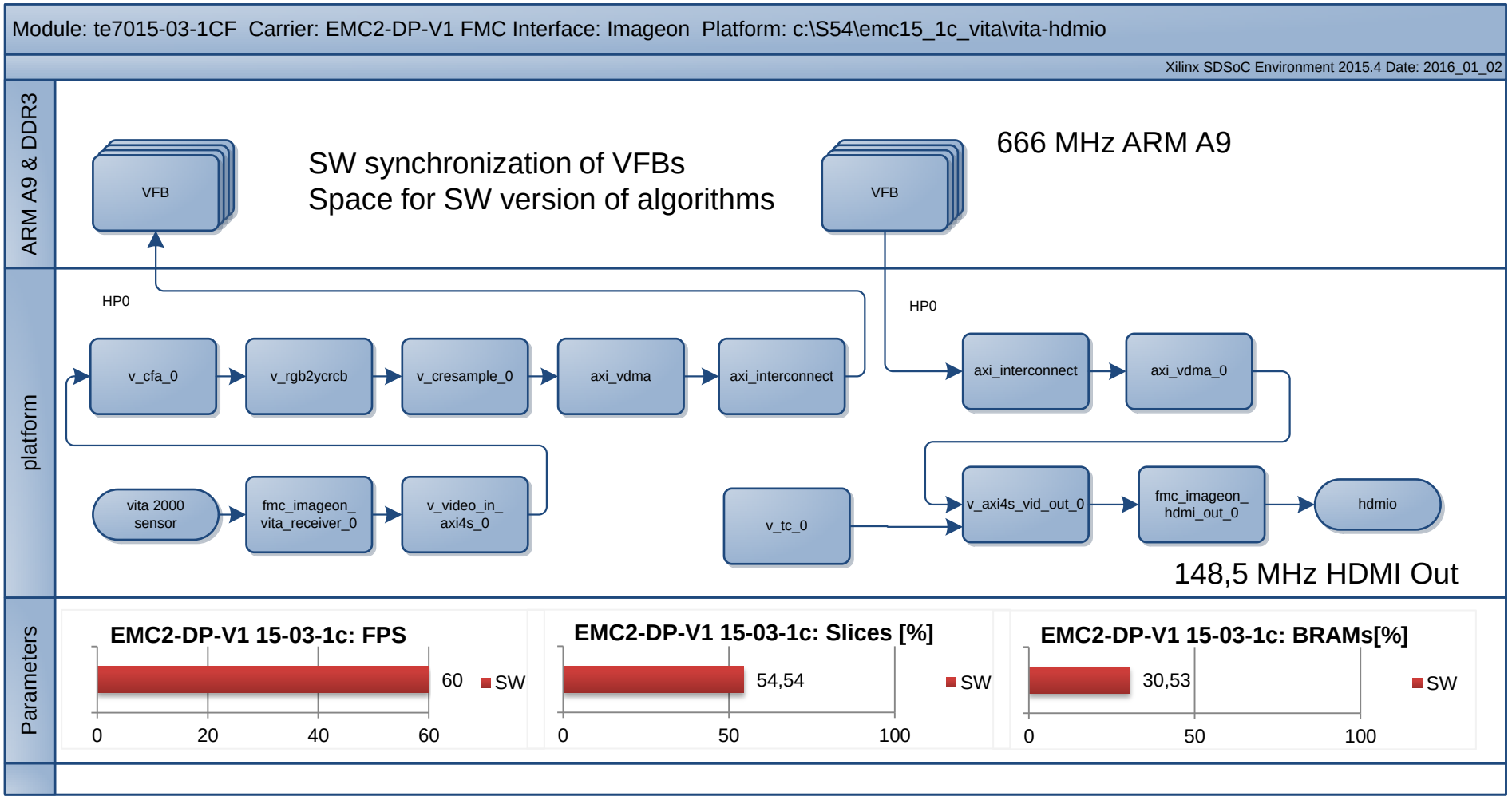
Motion Detection in Full HD Pf: HDMI In/Out
Process complete frame
Single computing data path in HW



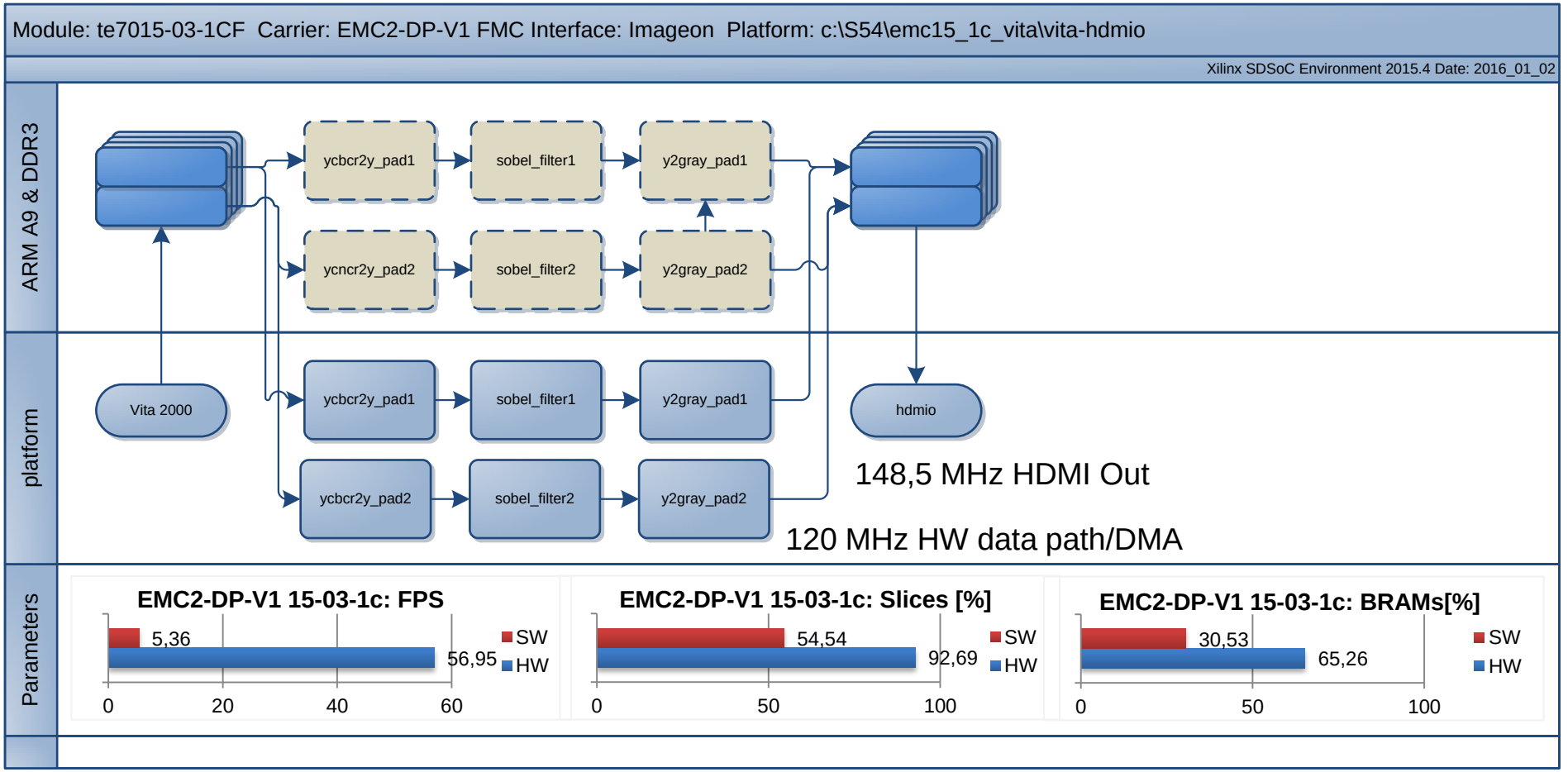
Motion Detection Full HD Pf: HDMI In/Out SW and HW flow in Xilinx SDSoC 2015.4 Carrier: EMC²-DP



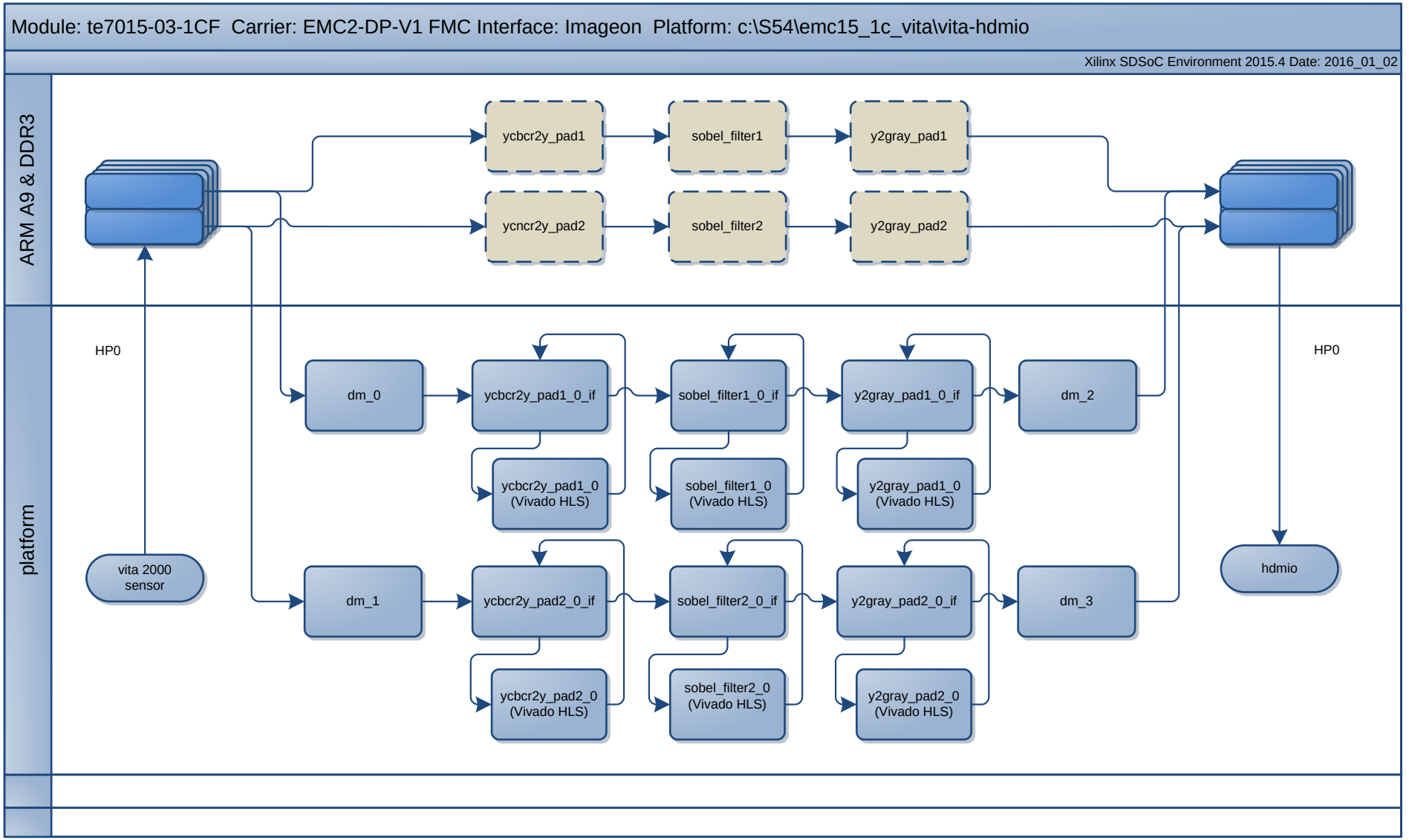
EMC²-DP with Vita Camera In/HDMI Out using SDSoC 2015.4 environment



Sobel filter in Full HD Pf: vita-hdmio
Process upper and lower part of frames
Two parallel computing data paths in HW



Sobel filter in Full HD Pf: Vita In/HDMI Out
Process upper and lower part of frames
Two parallel computing data paths in HW



Conclusions

Compile times in SDSoC (average laptop figures):

- SW: 1 min
- HW (Vivado IP Integrator System): 3 min
- HW (to bitstream and SD card BOOT.BIN): 60 min
- SDK (final SW project with HW accelerator): 1 min

Licensing:

- Xilinx is selling license of SDSoC
  (it is for all ZYNQ devices with Vivado and HLS)
- SDK (final SW project with HW accelerator): free

Acknowledgement: UTIA and Sundance are partially supported by the Artemis EMC2 project.