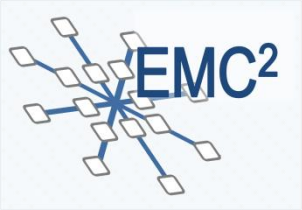


Xilinx SDSoC for Acceleration of Real-time Video Processing on 'COTS' ZYNQ Modules.

HiPEAC EMC2 Workshop – 2016-01-20

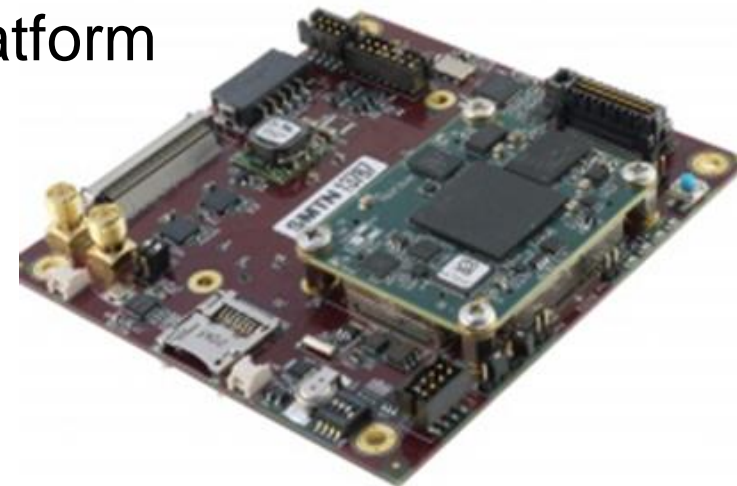
**Jiří Kadlec, Zdeněk Pohl, Lukáš Kohout
(UTIA AV ČR v.v.i. - Prague, Czech Republic)**

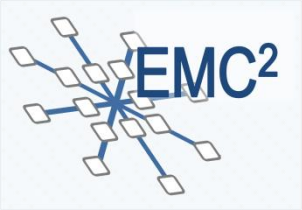
**Flemming Christensen, Mark Honman,
(Sundance - Chesham, United Kingdom)**



Introduction and Content

- Introduction to the Xilinx SDSoC Environment
- UTIA SDSoC 2015.4 HW Platform for **EMC²**-DP
 - HDMI-in – HDMI-out Demos
 - VITA Video Sensor-in HDMI-out Demos,
 - Data movers and HLS blocks
- Sundance's **EMC²** Development Platform

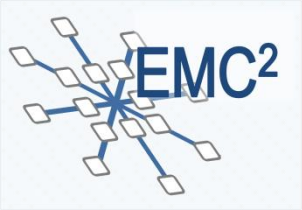




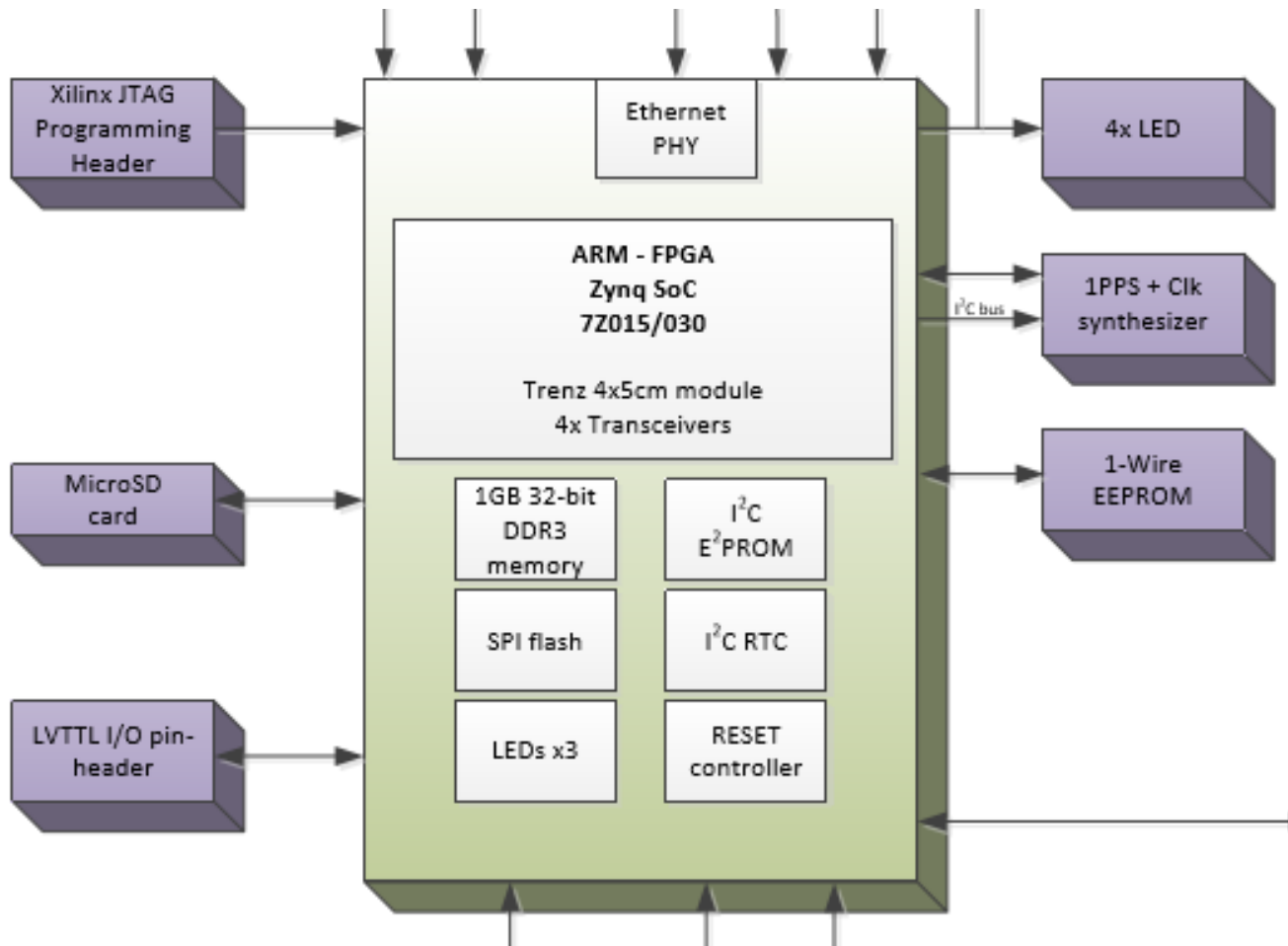
EMC² - System on Module

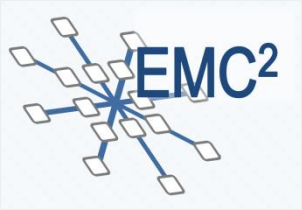


40mm x 50mm
Xilinx SoC or FPGAs
Zynq, Artix-7 or Kintex-7



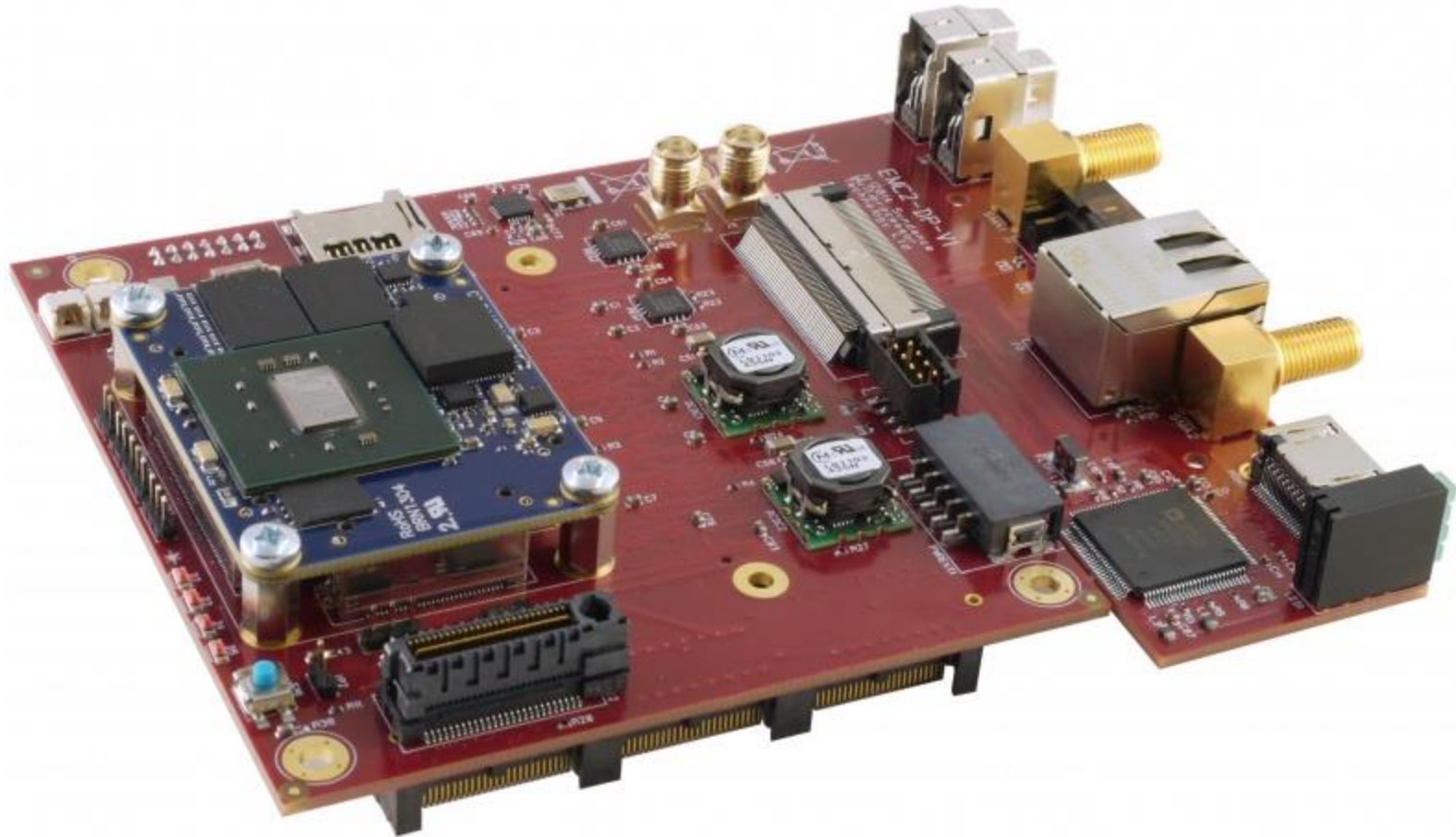
EMC² - System on Module

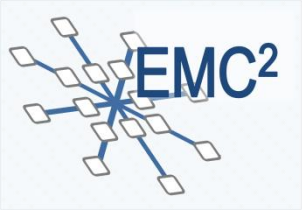




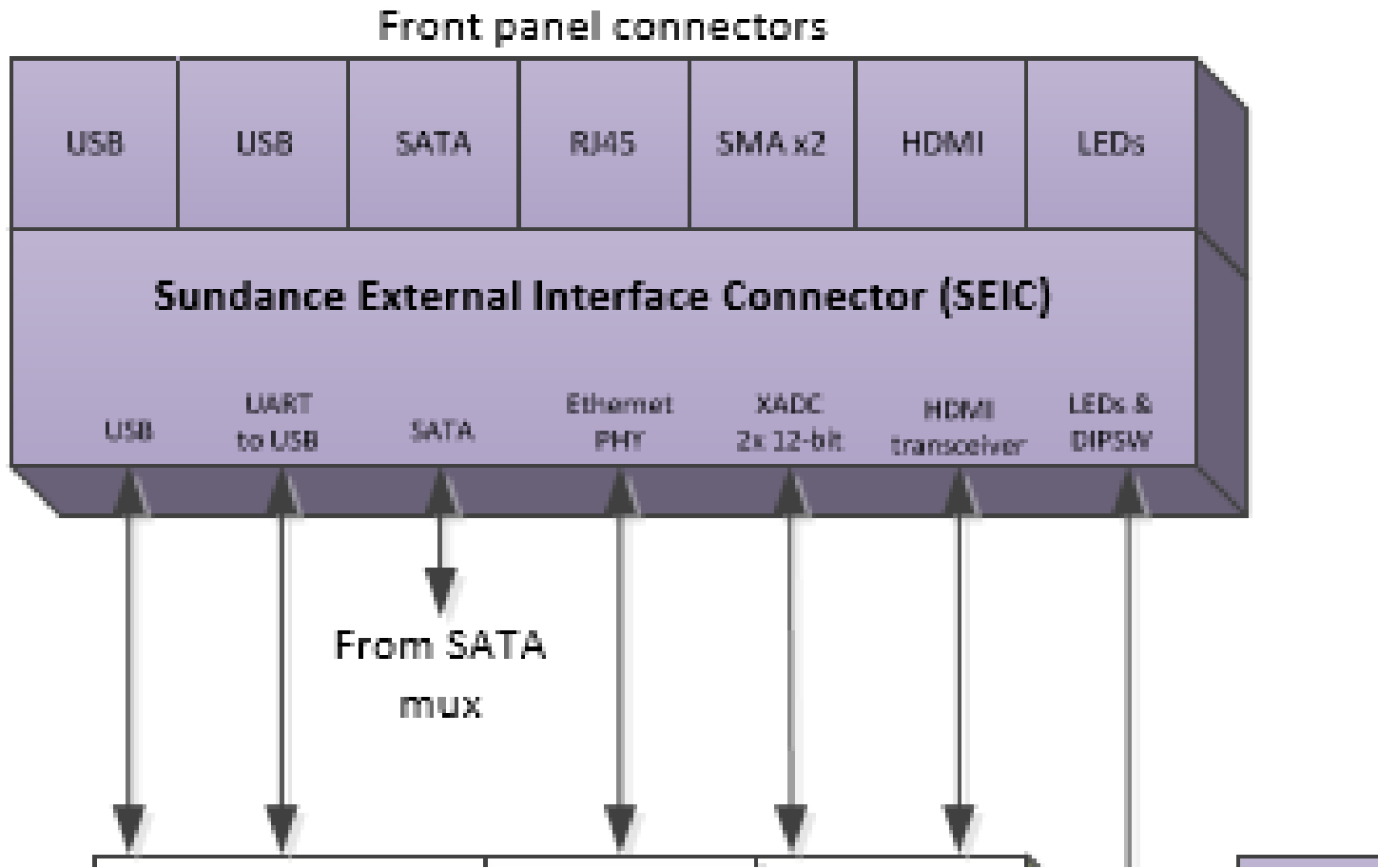
EMC² - Development Platform ,PC/104 Stackable Board`

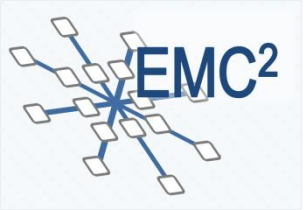
SUNDANCE



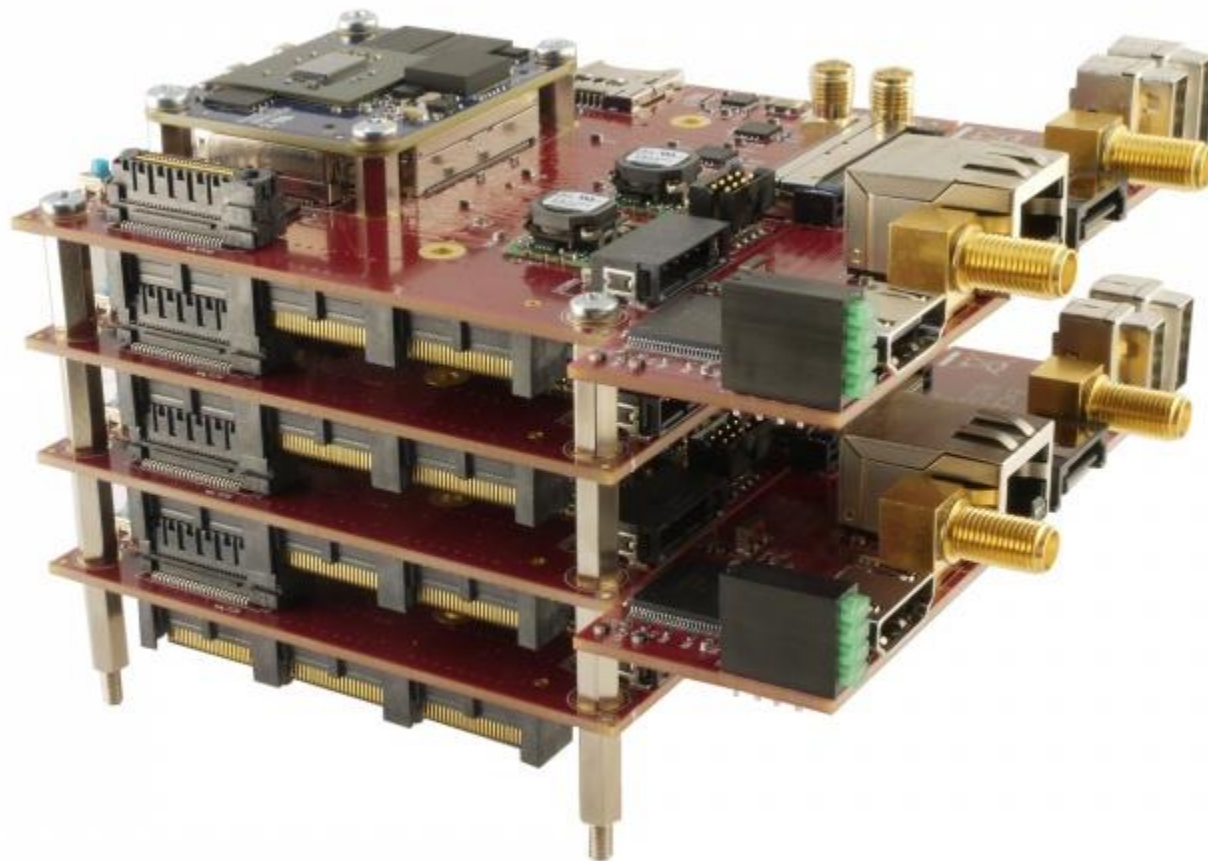


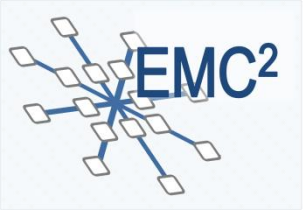
EMC² - Development Platform ,PC/104 Stackable Board` - IO Module



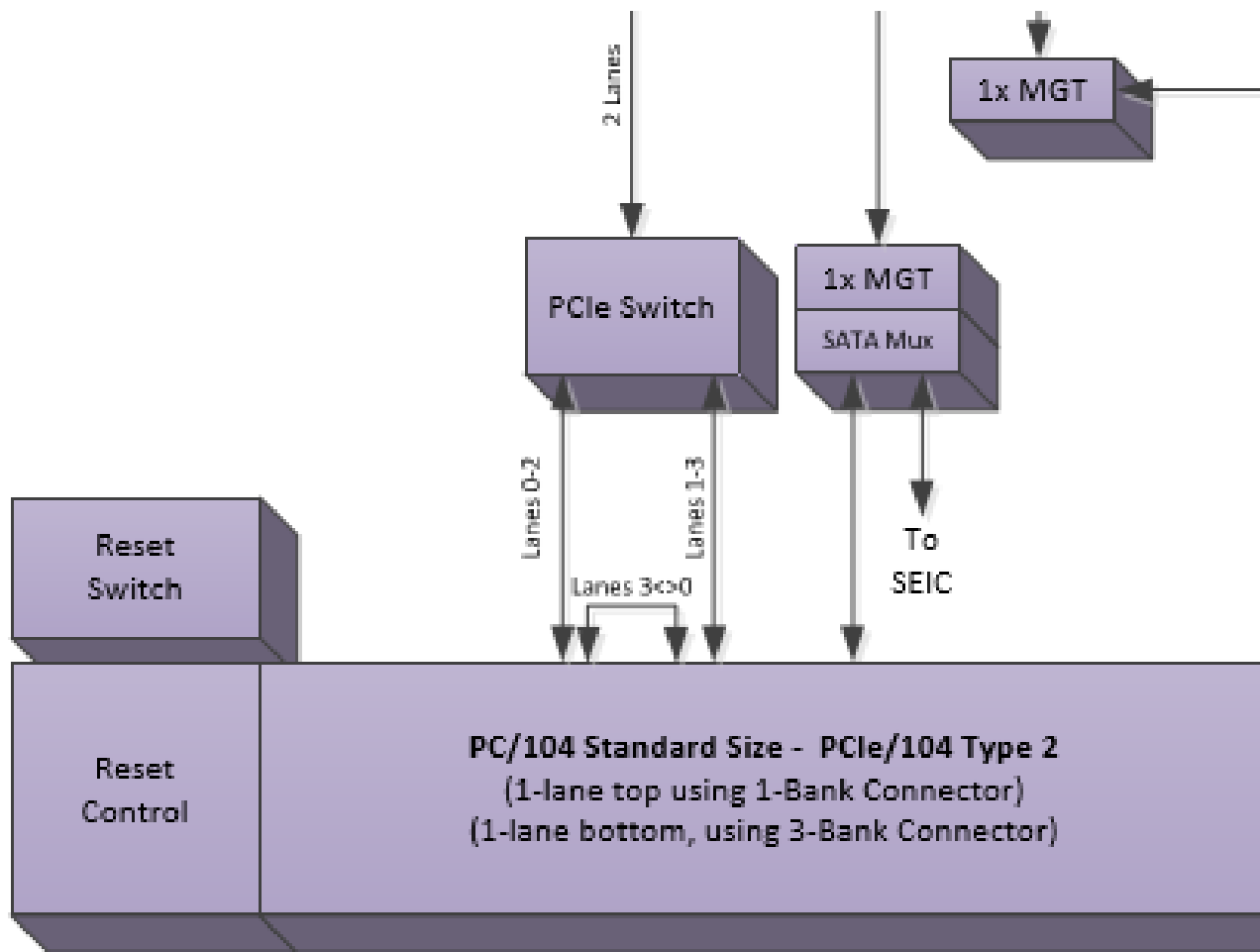


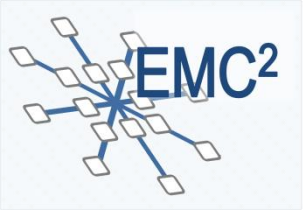
EMC² - Development Platform ,PC/104 Multiprocessing Stack`



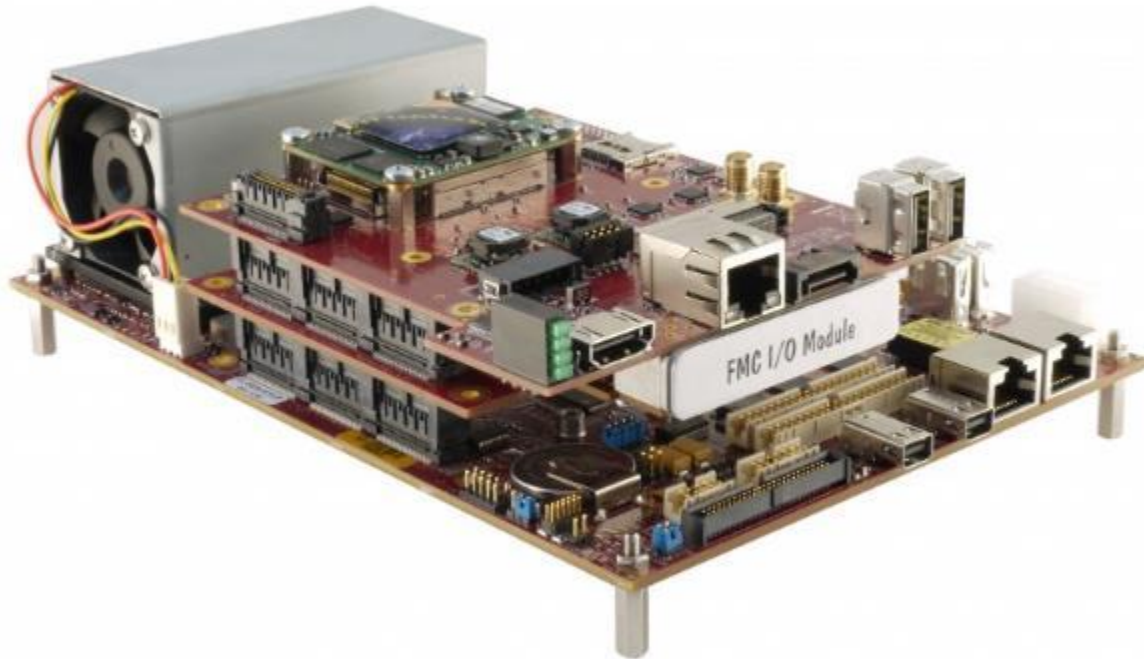


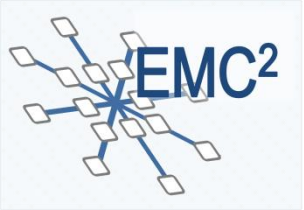
EMC² - Development Platform ,PC/104 Multiprocessing Stack`



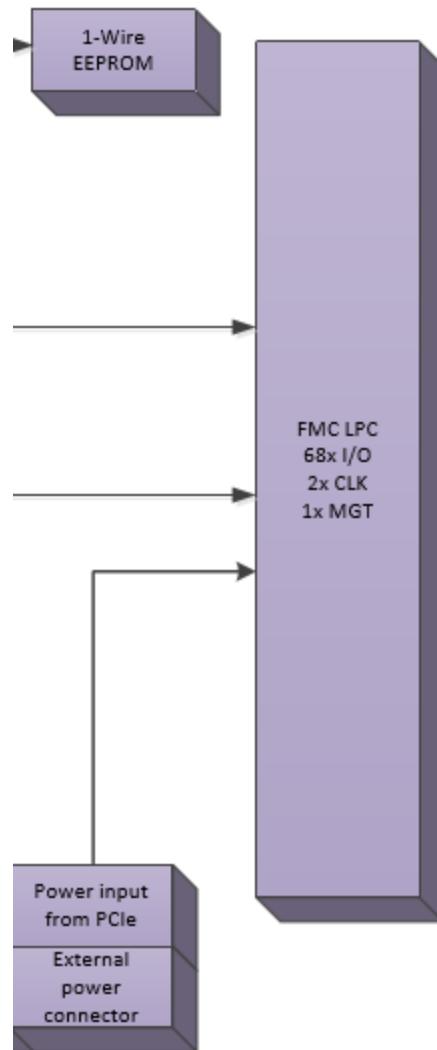


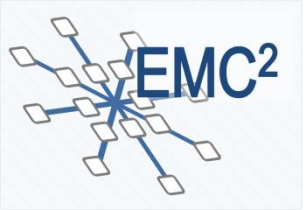
EMC² - Development Platform ,PC/104 I/O FMC Expansion Module`





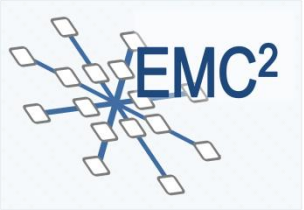
EMC² - Development Platform ,PC/104 I/O FMC Expansion Module`





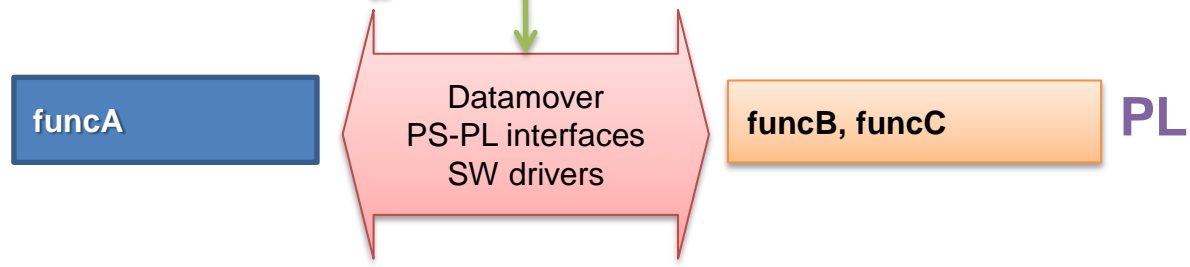
EMC² Video Processing Demo Xilinx SDSoC Environment



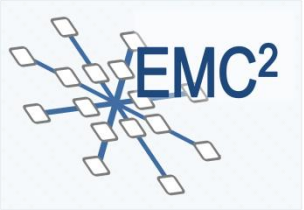


All Programmable SoCs Development Flow

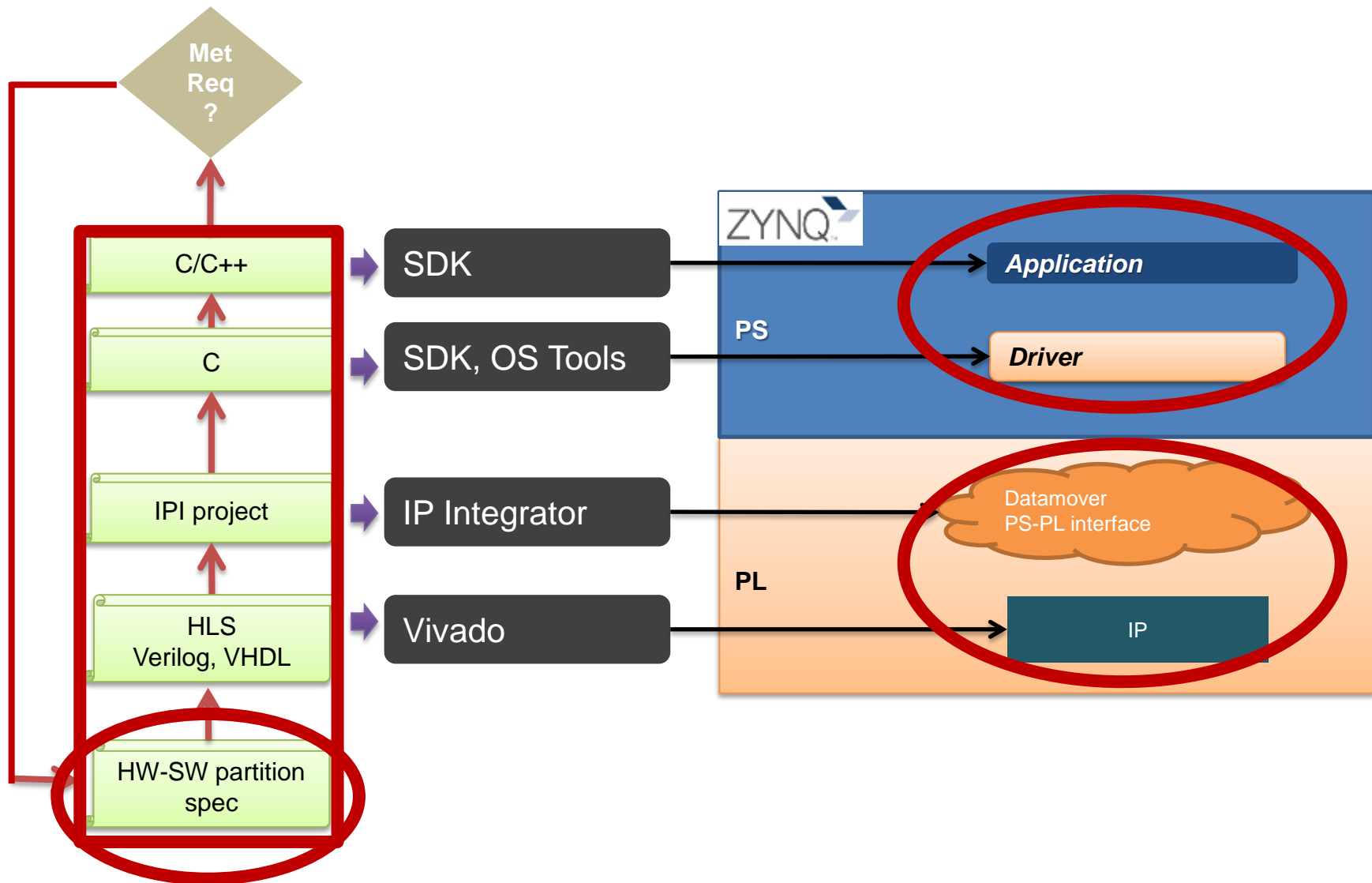
```
APP () {  
  funcA ();  
  funcB ();  
  funcC (); }
```

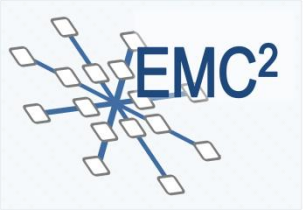


Explore optimal architecture

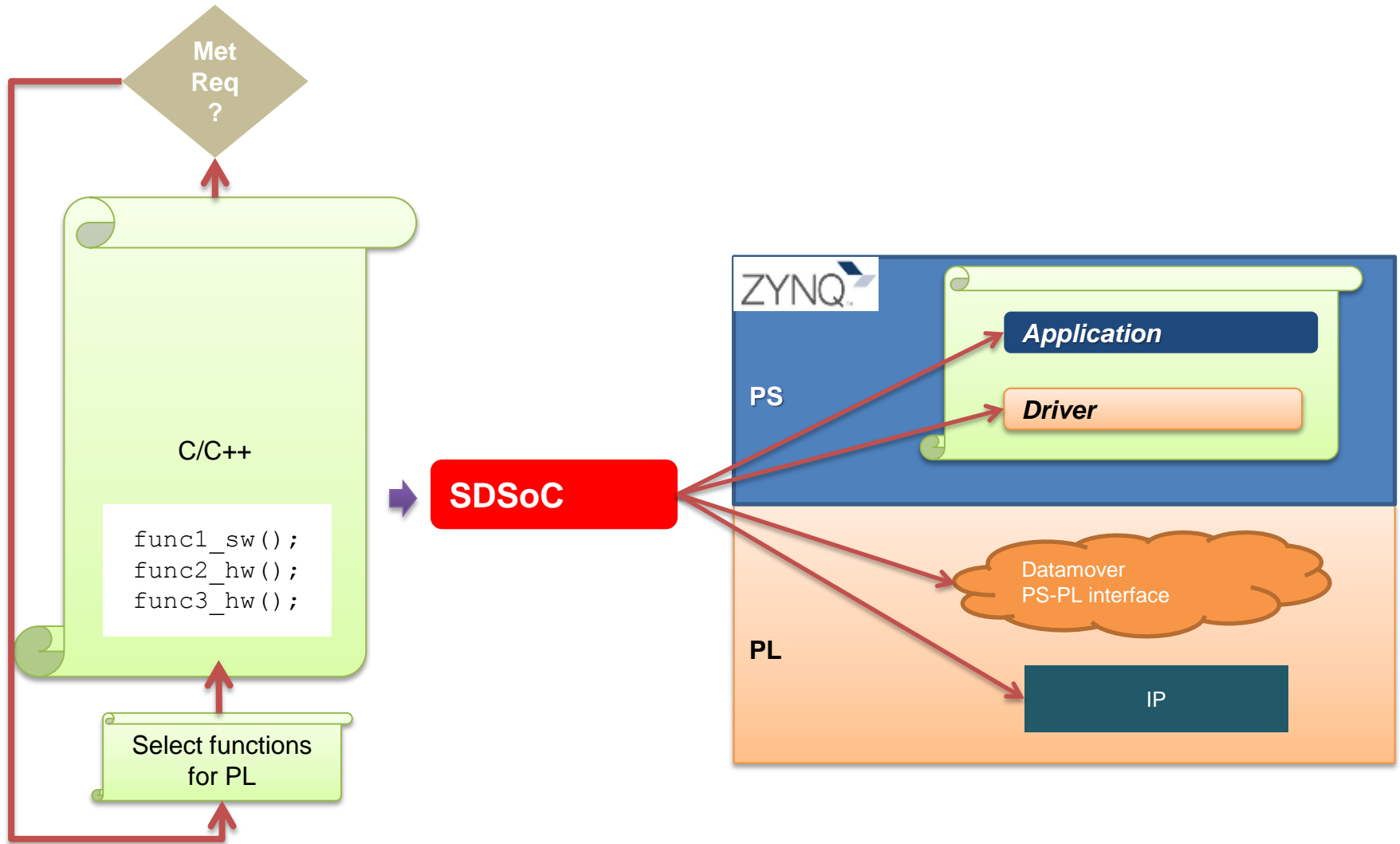


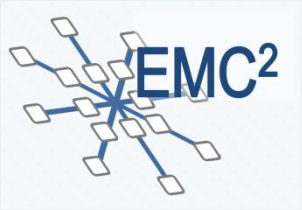
Without SDSoC: HW-SW Partition Exploration





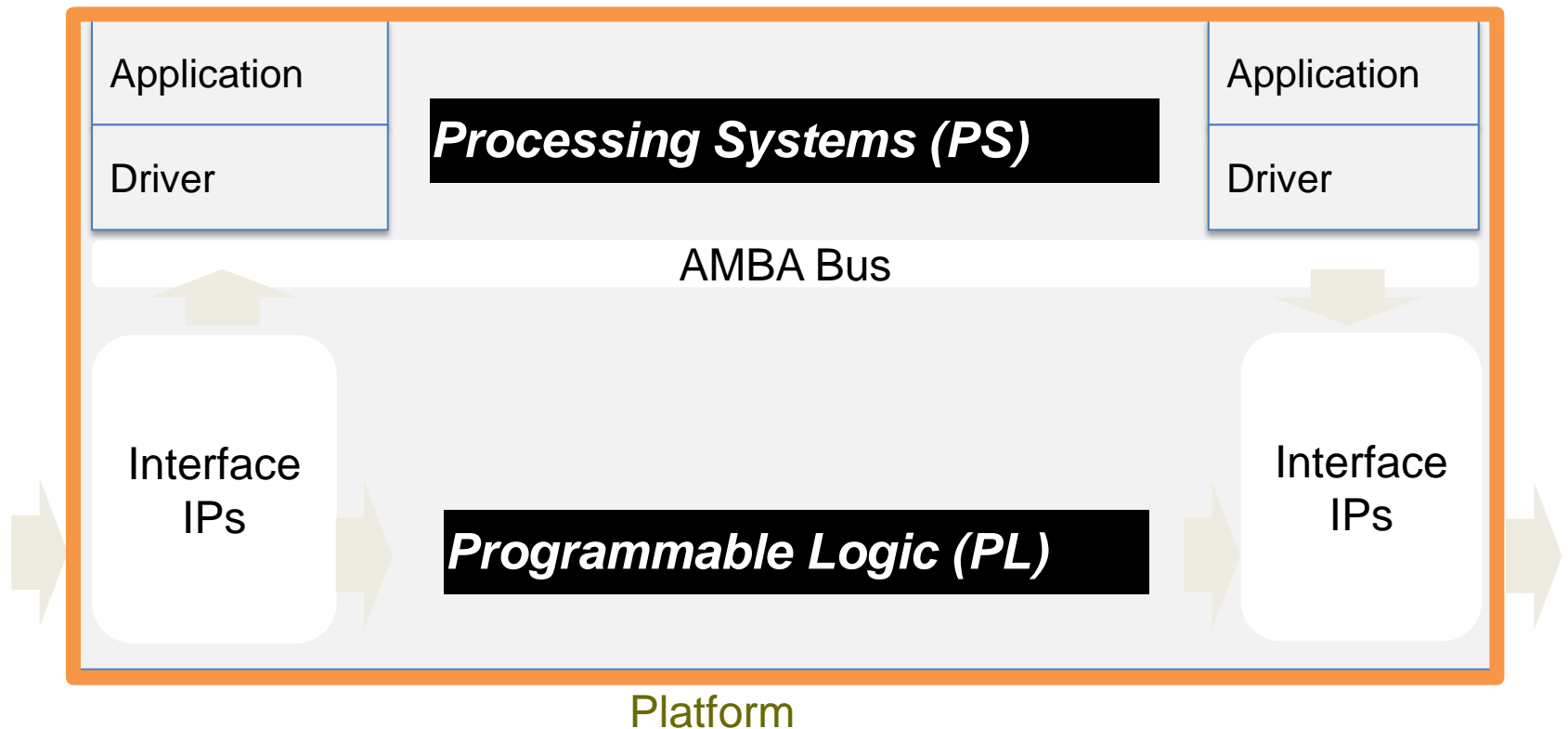
With SDSoC: Automatic System Generation

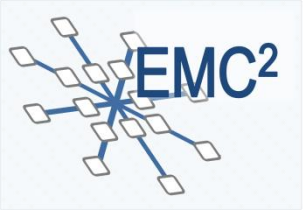




Base HW Platform for SDSoC

- Custom platform = Vivado project + Bootable software image
- Available for commonly used development kit and SoMs





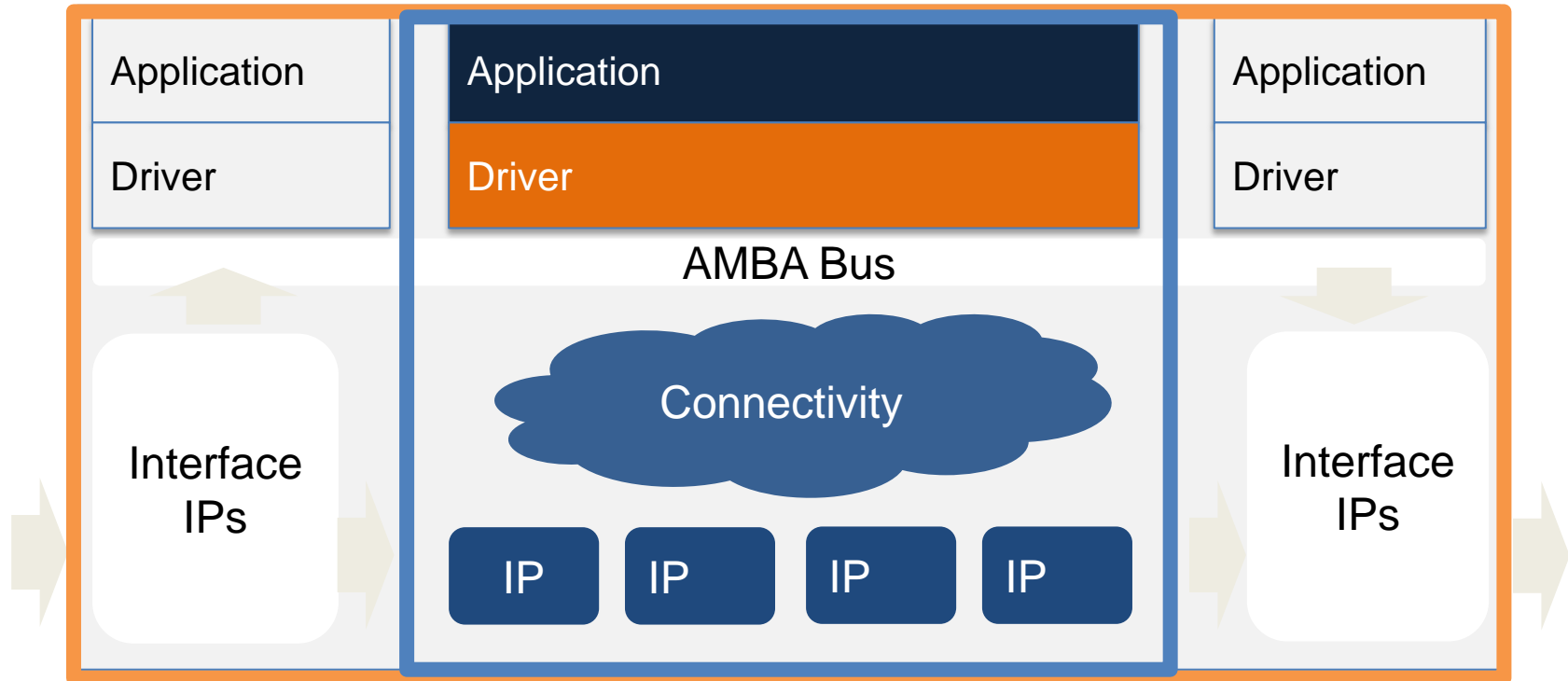
Complete SDSoC flow

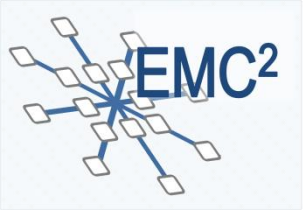
C/C++ Application



SDSoC Environment

Generated





SDSoC Example: Matrix Multiply +Add



C-callable IP

```

madd(inA,inB,out) {
    HDL IP
}

```

```

main() {
    malloc(A,B,C);
    mmult(A,B,D);
    madd(C,D,E);
    printf(E);
}

```

```

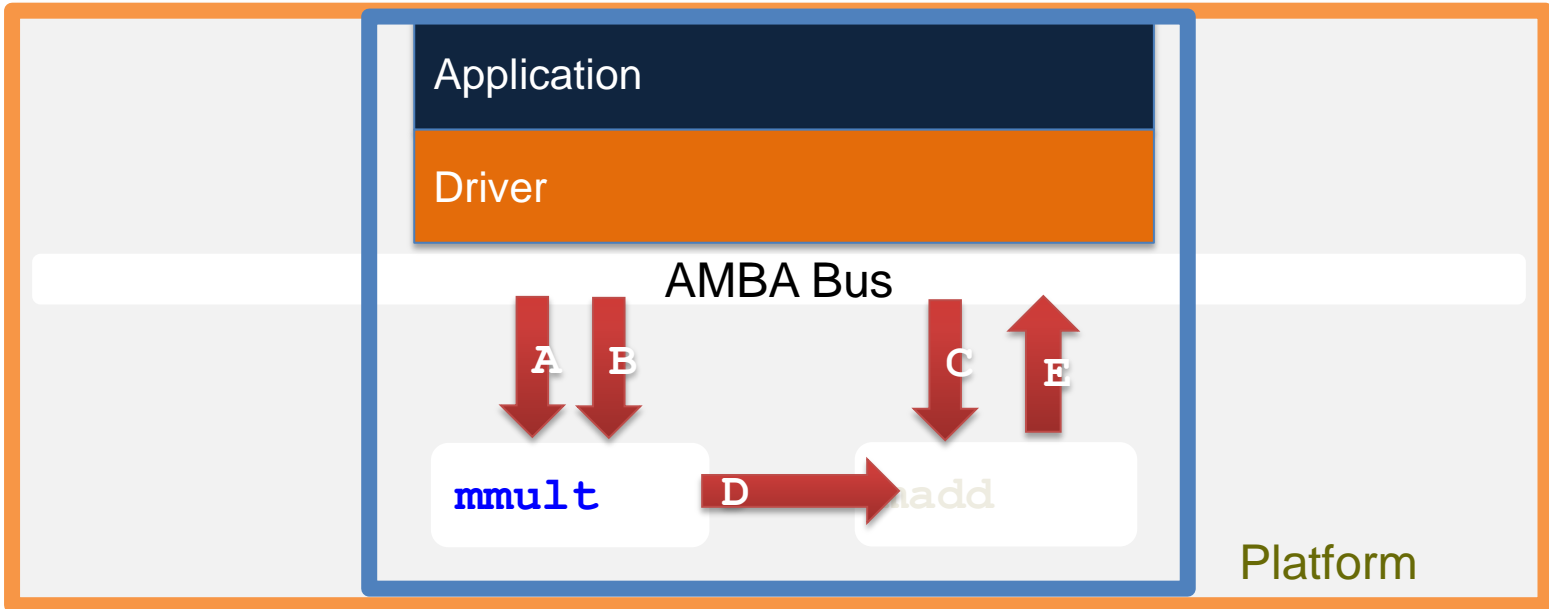
mmult(inA,inB,out) {
    HLS C/C++
}

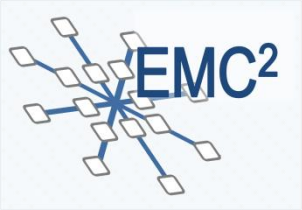
```



A, B datamovers

Generated





EMC² – DP w. HDMI In/Out FMC Module running SDSoC 2015.4 environment



Module: te7015-03-1CF Carrier: EMC2-DP-V1 FMC Interface: Imageon Platform: c:\S54\emc15_1c_hdmi\hdmi-hdmi

Xilinx SDSoC Environment 2015.4 Date: 2016_01_02

ARM A9 & DDR3

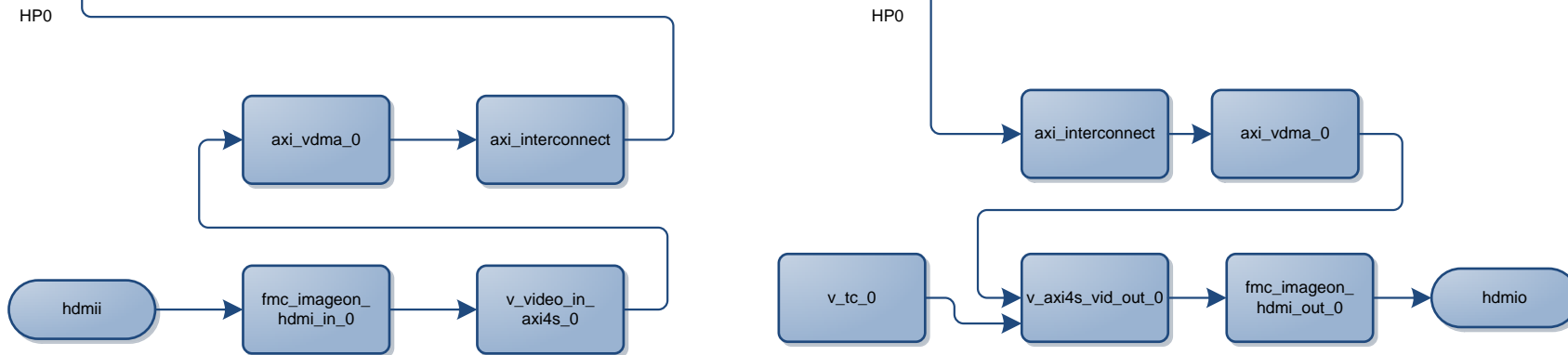


SW synchronization of VFBs
Space for SW version of algorithms

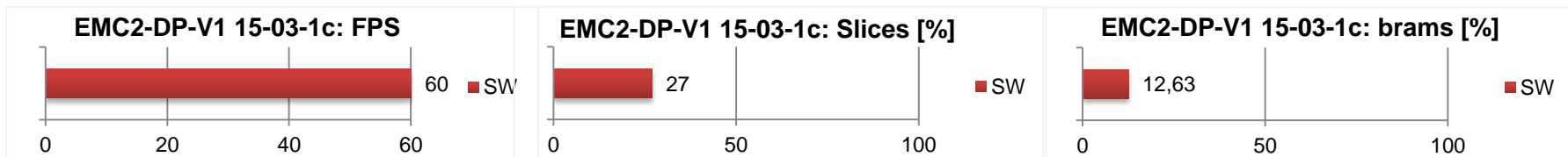


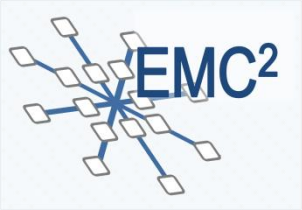
666 MHz ARM A9

platform



Parameters





Sobel Filter Full HD Pf: HDMI In/Out

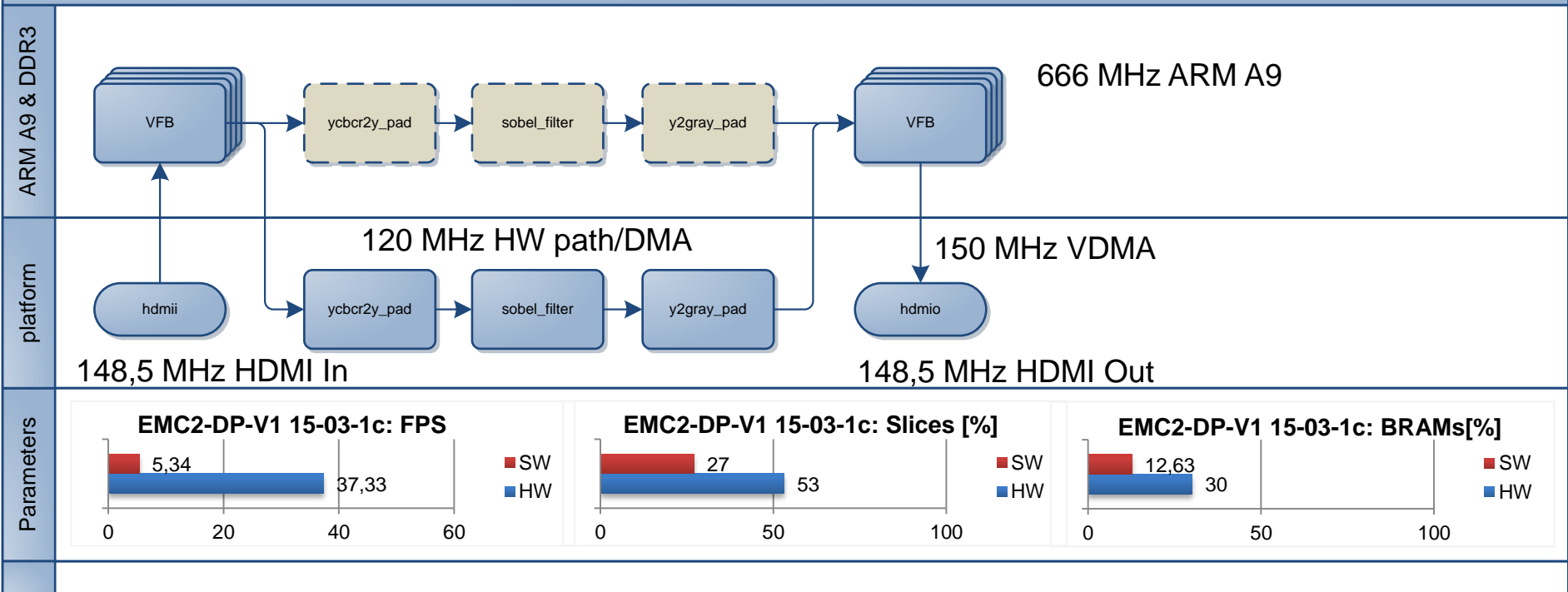
SW and HW flow in Xilinx SDSoC 2015.4

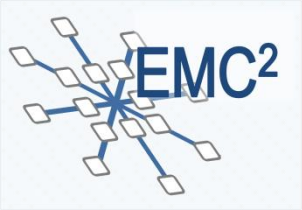
Carrier: EMC2-DP



Module: te7015-03-1CF Carrier: EMC2-DP-V1 FMC Interface: Imageon Demo_SW: so01 Demo_HW so02 Platform: c:\S54\emc15_1c_hdmi\hdmi-hdmi

Xilinx SDSoC Environment 2015.4 Date: 2016_01_02





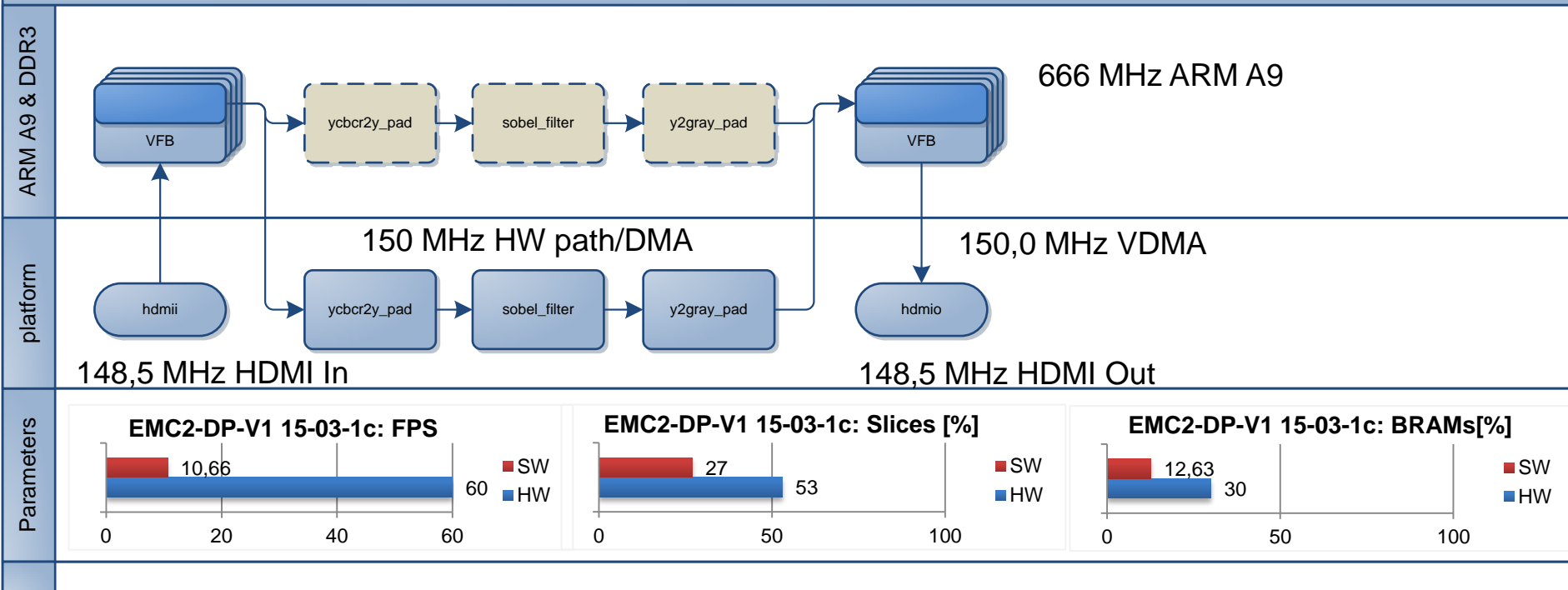
Sobel Filter Full HD Pf: HDMI In/Out

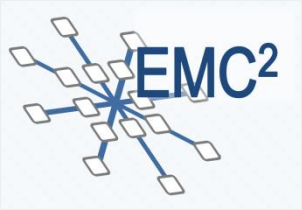
Process only upper 50% of frames
Single computing data path in HW



Module: te7015-03-1CF Carrier: EMC2-DP-V1 FMC Interface: Imageon Demo_SW: so03 Demo_HW so04 Platform: c:\S54\emc15_1c_hdmi\hdmi-hdmi

Xilinx SDSoC Environment 2015.4 Date: 2016_01_02





Sobel filter in Full HD Pf: HDMI In/Out

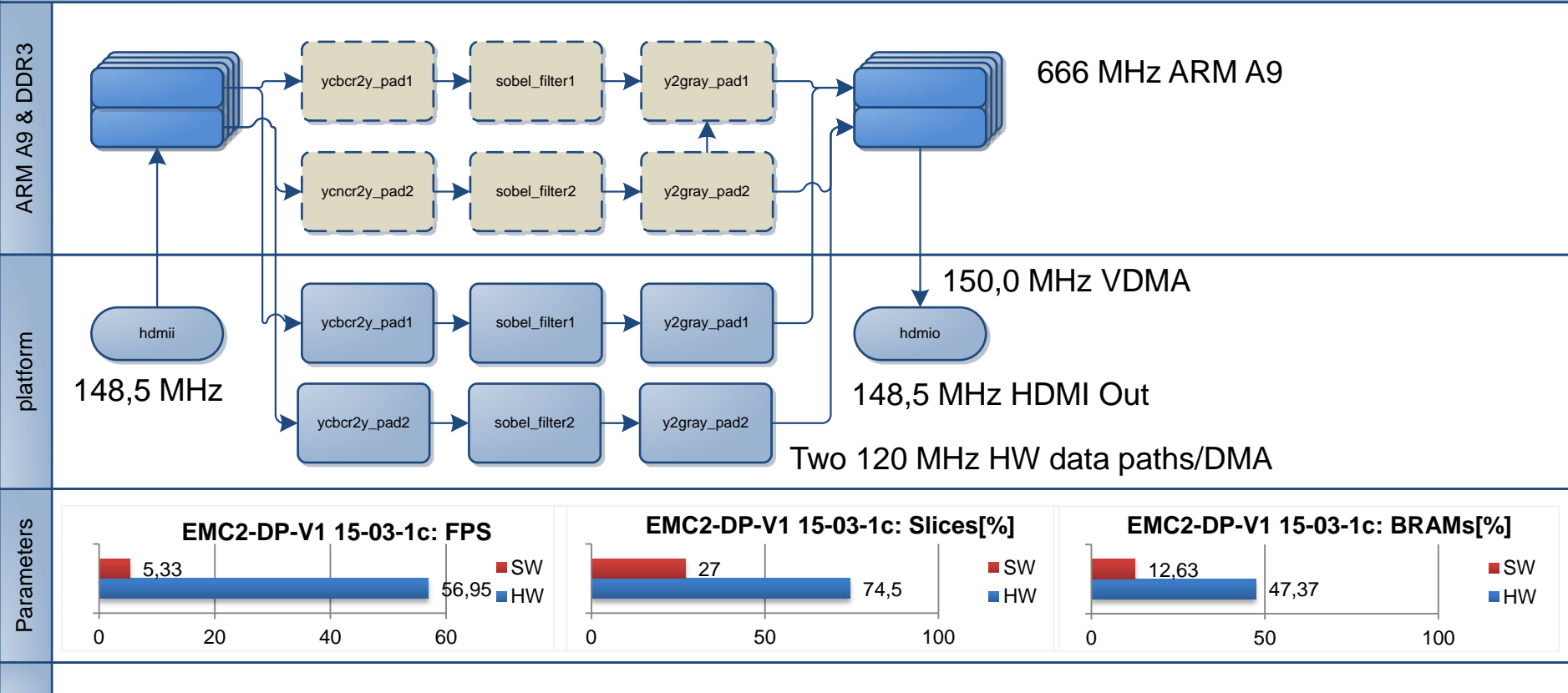
Process upper and lower part of frames

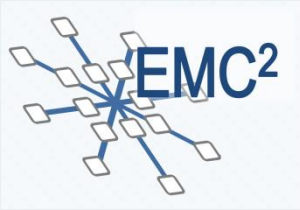
Two parallel computing data paths in HW



Module: te7015-03-1CF Carrier: EMC2-DP-V1 FMC Interface: Imageon Demo_SW: so05 Demo_HW so06 Platform: c:\S54\emc15_1c_hdmi\hdmi-hdmi

Xilinx SDSoC Environment 2015.4 Date: 2016_01_02





Motion Detection in Full HD Pf: HDMI In/Out

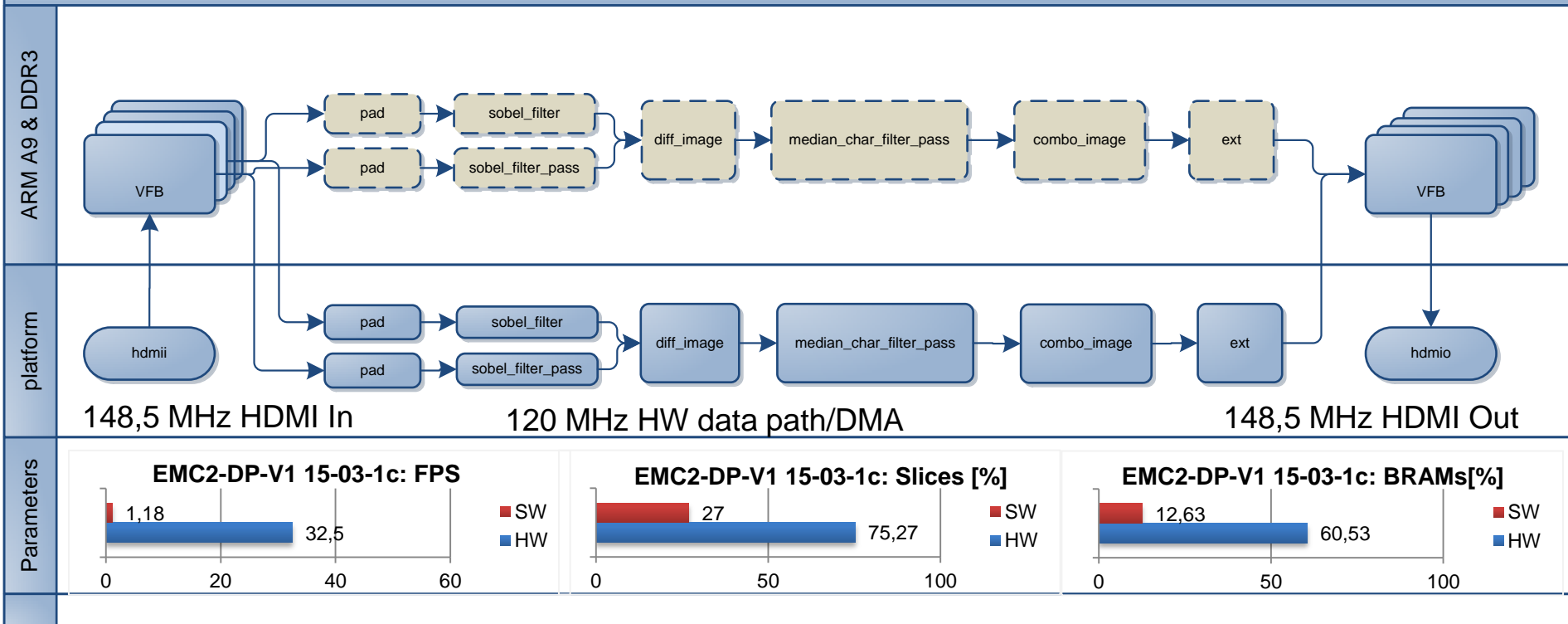
Process complete frame

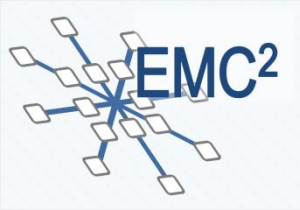
Single computing data path in HW



Module: te7015-03-1CF Carrier: EMC2-DP-V1 FMC Interface: Imageon Demo_SW: md01 Demo_HW md02 Platform: c:\S54\emc15_1c_hdmi\hdmii-hdmio

Xilinx SDSoC Environment 2015.4 Date: 2016_01_02



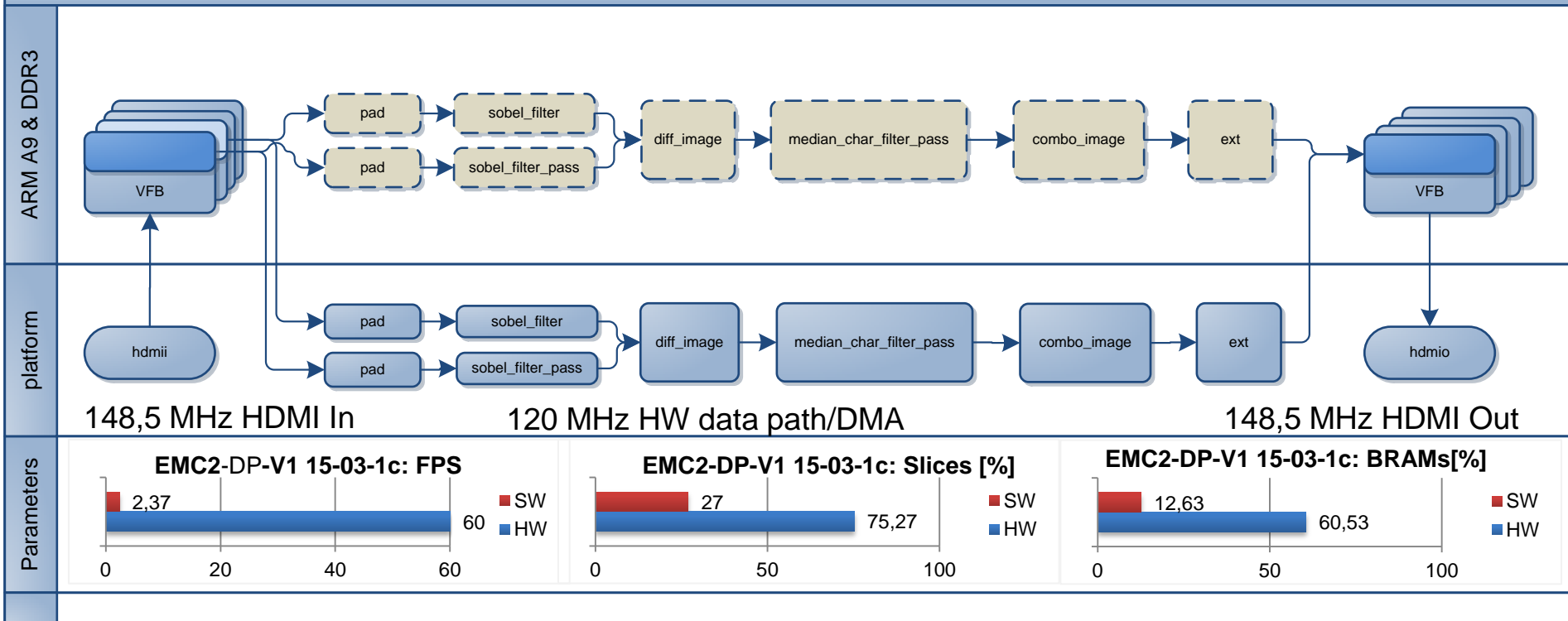


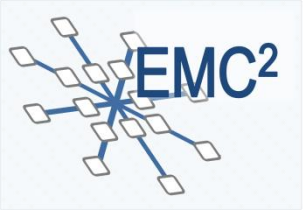
Motion Detection Full HD Pf: HDMI In/Out SW and HW flow in Xilinx SDSoC 2015.4 Carrier: EMC²-DP



Module: te7015-03-1CF Carrier: EMC2-DP-V1 FMC Interface: Imageon Demo_SW: md03 Demo_HW md04 Platform: c:\S54\emc15_1c_hdmi\hdmii-hdmio

Xilinx SDSoC Environment 2015.4 Date: 2016_01_02





EMC²-DP with Vita Camera In/HDMI Out using SDSoC 2015.4 environment



Module: te7015-03-1CF Carrier: EMC2-DP-V1 FMC Interface: Imageon Platform: c:\S54\emc15_1c_vita\vita-hdmio

Xilinx SDSoC Environment 2015.4 Date: 2016_01_02

ARM A9 & DDR3

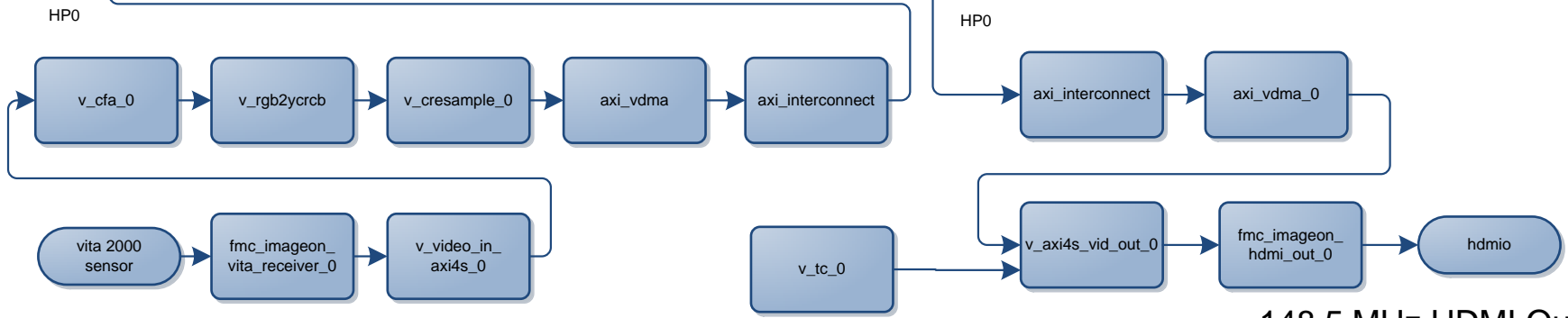


SW synchronization of VFBs
Space for SW version of algorithms



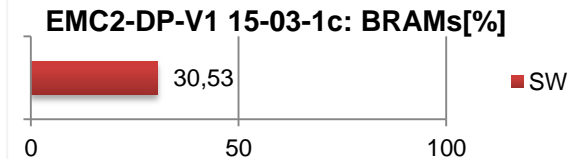
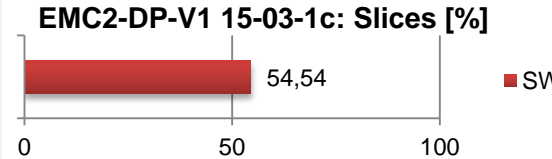
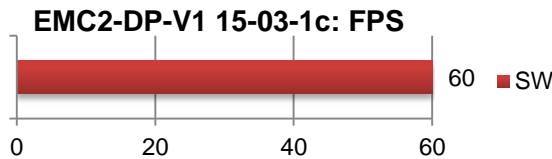
666 MHz ARM A9

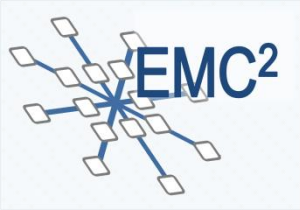
platform



148,5 MHz HDMI Out

Parameters





Sobel filter in Full HD Pf: vita-hdmio

Process upper and lower part of frames

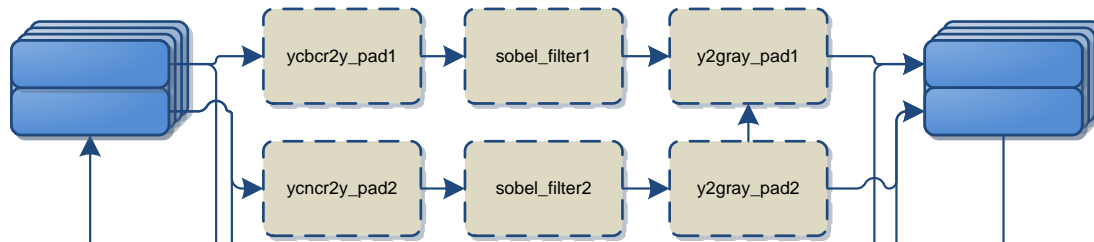
Two parallel computing data paths in HW



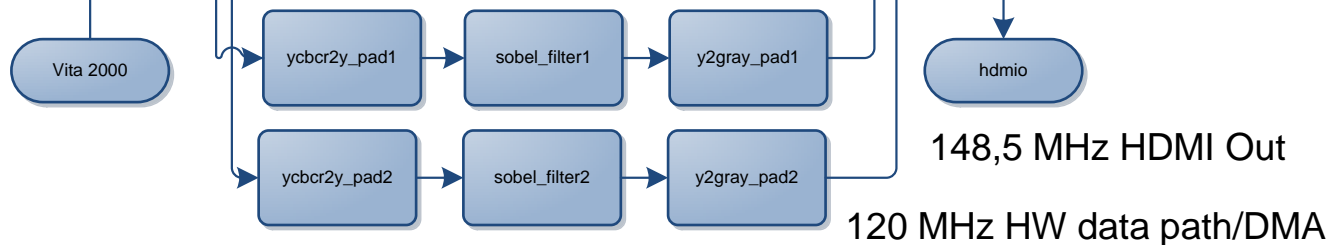
Module: te7015-03-1CF Carrier: EMC2-DP-V1 FMC Interface: Imageon Platform: c:\S54\emc15_1c_vita\ vita-hdmio

Xilinx SDSoC Environment 2015.4 Date: 2016_01_02

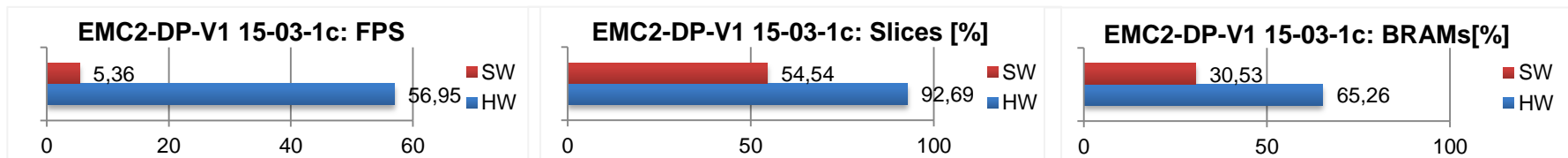
ARM A9 & DDR3

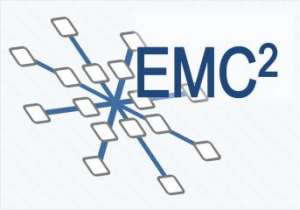


platform



Parameters





Sobel filter in Full HD Pf: Vita In/HDMI Out

Process upper and lower part of frames

Two parallel computing data paths in HW

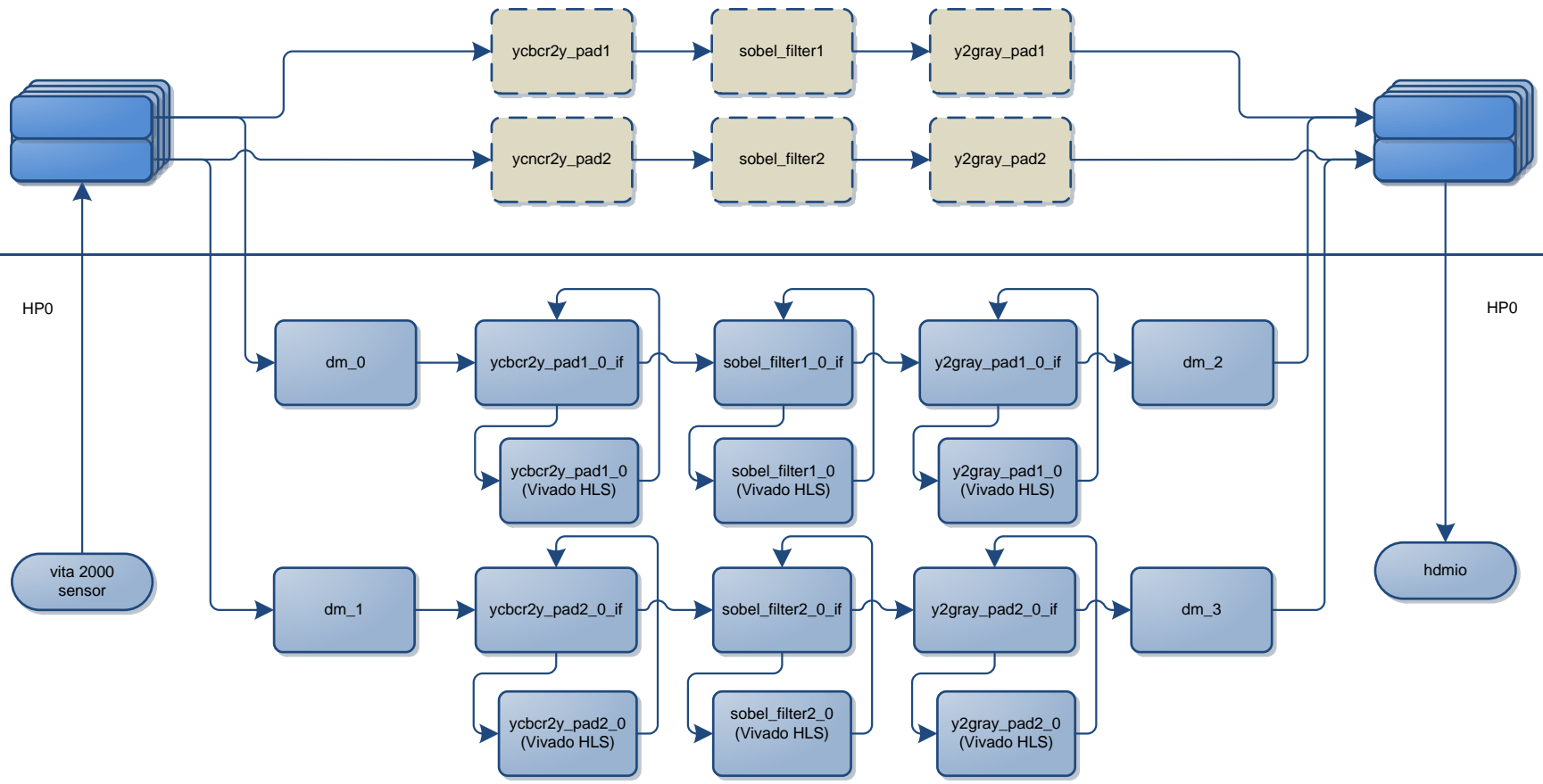


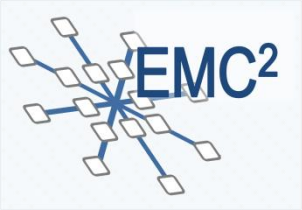
Module: te7015-03-1CF Carrier: EMC2-DP-V1 FMC Interface: Imageon Platform: c:\S54\emc15_1c_vita\vita-hdmio

Xilinx SDSoC Environment 2015.4 Date: 2016_01_02

ARM A9 & DDR3

platform





Conclusions

Compile times in SDSoC (average laptop figures):

- SW: 1 min
- HW (Vivado IP Integrator System): 3 min
- HW (to bitstream and SD card BOOT.BIN): 60 min
- SDK (final SW project with HW accelerator): 1 min

Licensing:

- Xilinx is selling license of SDSoC
(it is for all ZYNQ devices with Vivado and HLS)
- SDK (final SW project with HW accelerator): free

Acknowledgement: UTIA and Sundance are partially supported by the Artemis EMC2 project.