Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments

Demonstrator context & objectives

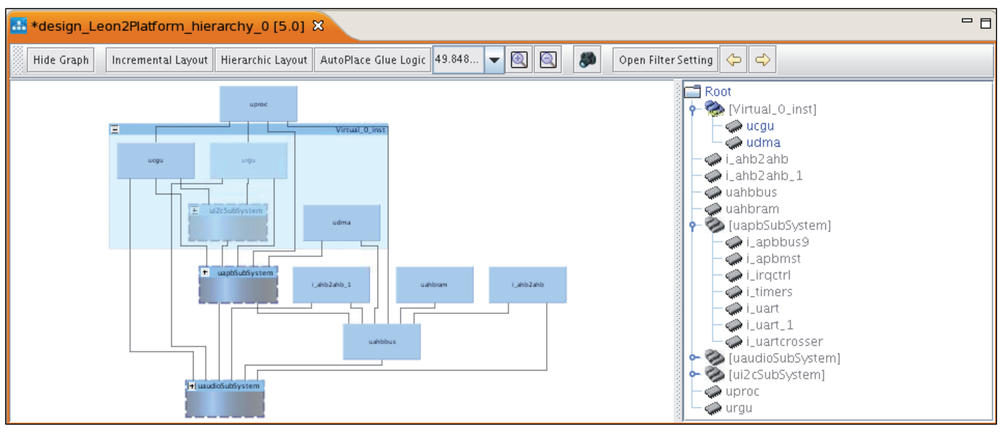
One of the major challenges faced by engineers during design of mixed-criticality multicore systems is to ensure 0the fulfilment of criticality levels of the various SW tasks. The verification and validation steps are particularly tedious when systems have to cope with dynamicity in terms of quality of services according to their various functional modes. The management of shared resources then becomes crucial and calls for methodologies to aguarantee the freedom of interference between tasks. We hereby address this topic with a tooled flow leveraging HW detailed characteristics for SW deployment.

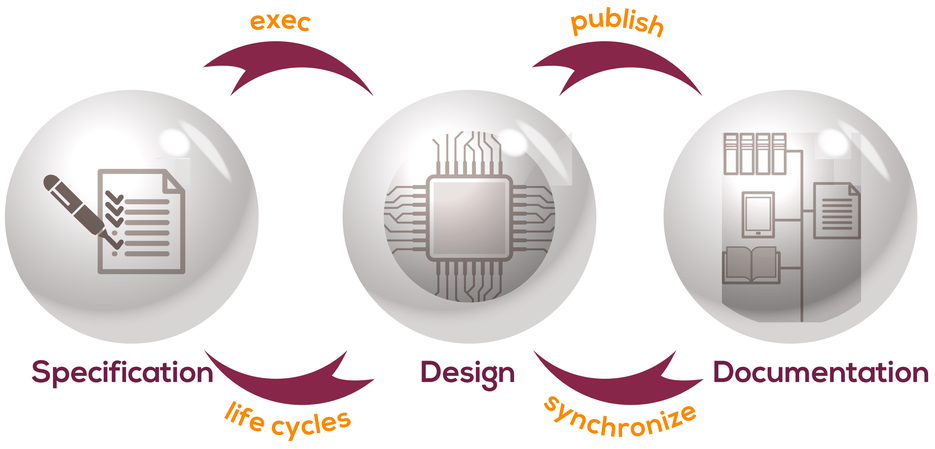
mRegister View & Virtual Hierarchy

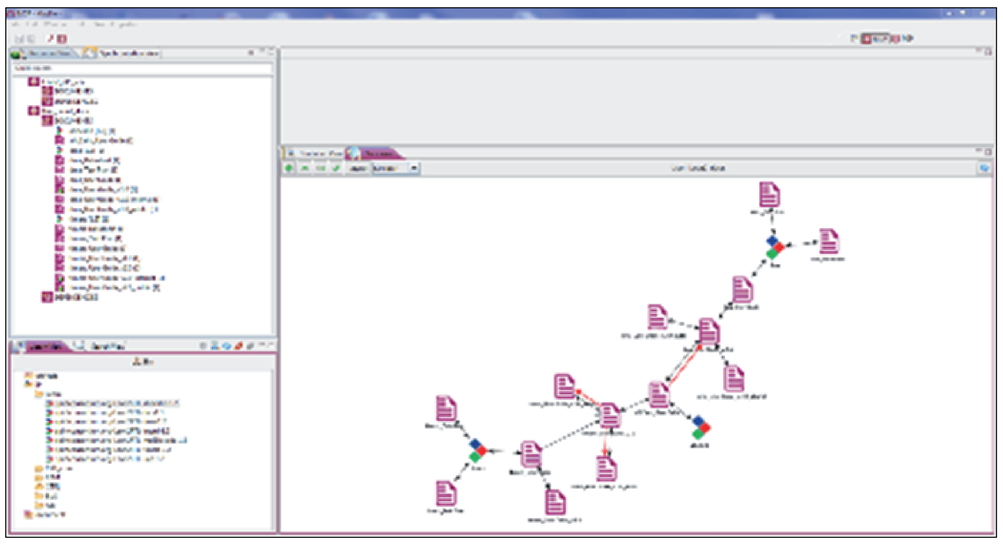
Magillem Register View (MRV) manages the detailed HW Design Description:

- Configurable IP registers (complete registers model)
- Detailed description of memory maps
- Specific information about HW characteristics (e.g. security levels, performances)

The application SW mapping intent is specified on as a virtual hierarchy on top of the HW model.



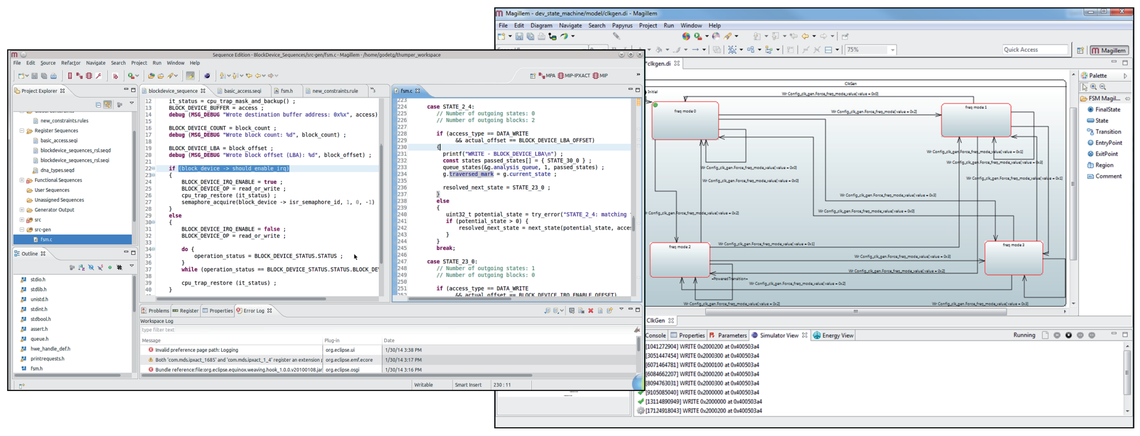




mSequence Editor

In Magillem Sequence Editor, SW sequences are expressed by leveraging the HW Design Description and the mapping, as virtual hierarchy.

- Three abstractions levels (IP, sub-functional, functional)
- Describes authorized access sequences
- Builds on HW-dependent SW layers
- Linked to the platform description (memory accesses)
- C-like syntax with a few exclusive additions



Integrated Specification, Design and Documentation (ISDD) flow

In combination, MRV and MSE provide effective means to go towards implementation by generating implementation code from access sequences, as well as the possibility to validate compliance of code with regards to the HW dynamicity, expressed as state diagrams linked to the defined sequences.

By integrating specification with design and documentation, this flow provides:

- traceability between the elements involved (requirements, SW tasks, HW resources, sequences)
- predefined templates of dependencies included in the tool
- support of existing de facto standards (ReqIF, IP-XACT, UML, Word, Excel)

Benefits of the proposed approach

- Full traceability (specification, design, documentation)
- Tight coupling between HW and SW
- Refined analysis of HW/SW interactions
- Integrated environment (Eclipse)
- Relies on industrial standards

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