ARTEMIS TECHNOLOGY CONFERENCE

EMC² Workshop

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WP4 Multi-core Hardware Architectures and Concepts

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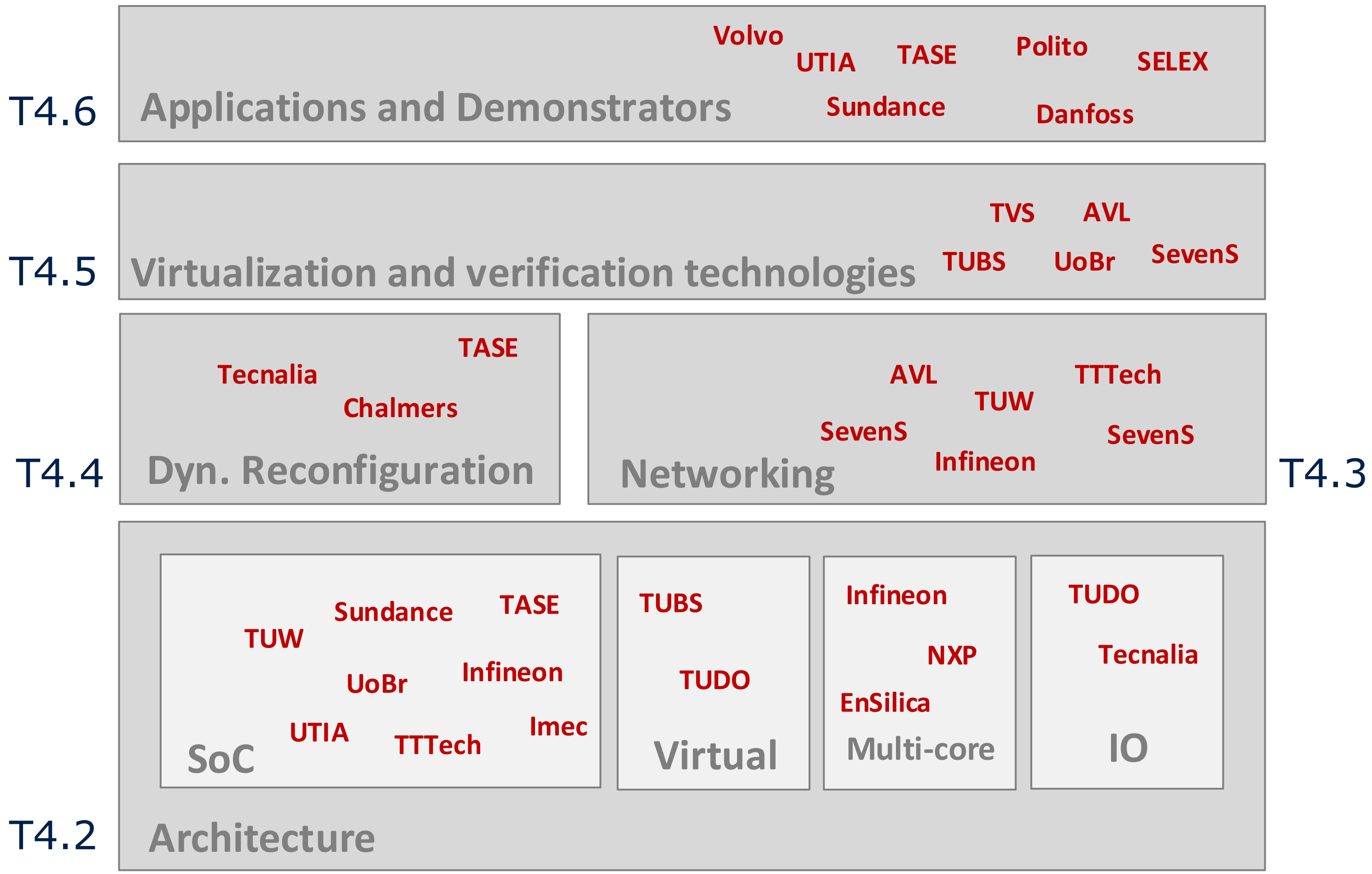
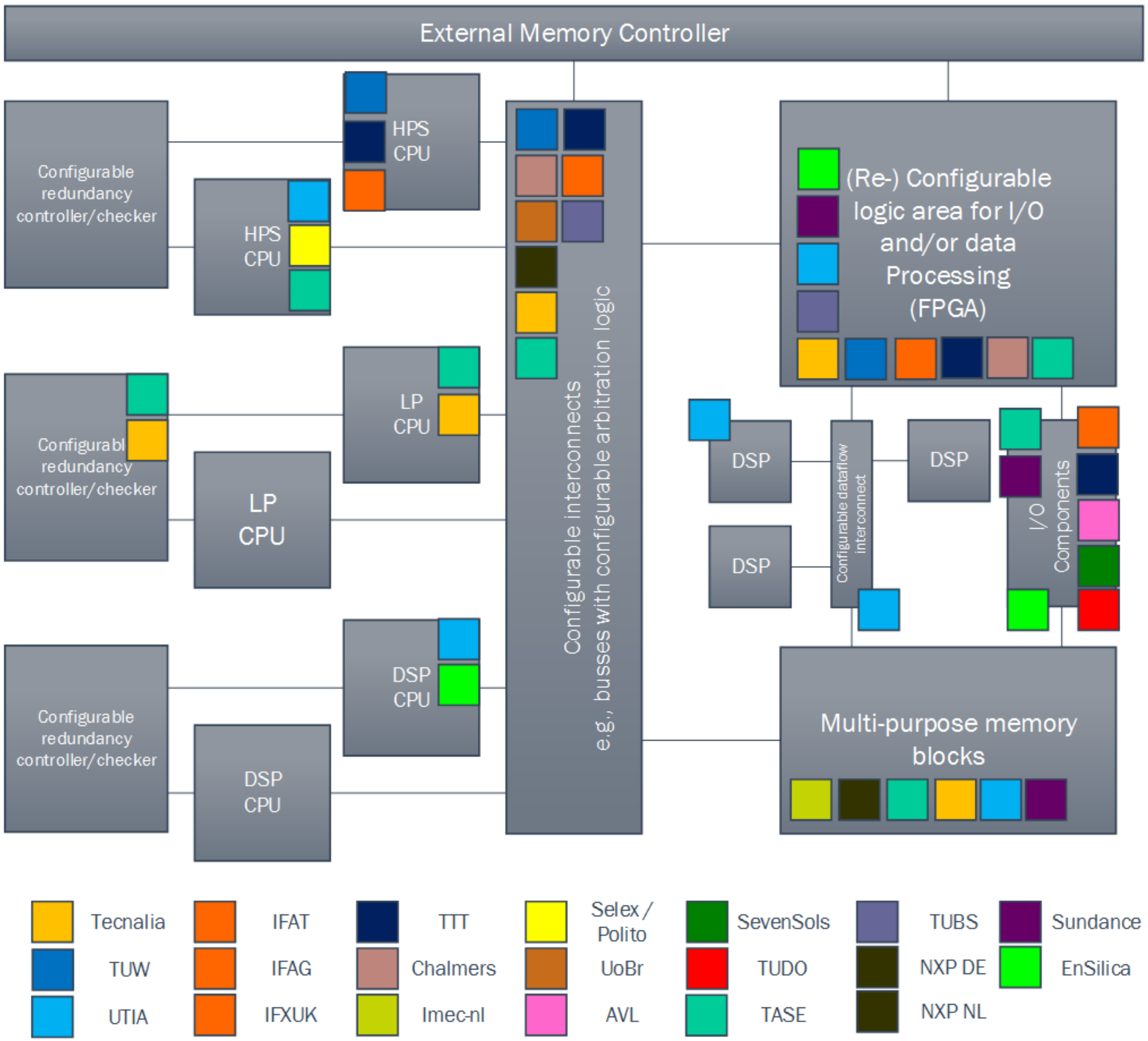
WP4 Architectures and Concepts
Agenda

- Technical Overview
- Objectives
- Highlights

Technical Overview
5 Technology Lanes



Technical Overview
Spread over System Segments



Objectives
Current phase

- Hardware platforms and tools applied **to internal use-cases**
- Ongoing **evaluation** and **knowledge transfer** of the proposed technologies and tools with other WPs and Living Labs

- Development of Hardware Technologies and Demonstrators following requirements and along Technology Lanes
- Evaluate interfaces to run-time (WP3) and Application Models/Tools (WP2)
- Evaluate Dissemination to LLs (WP12)

Technology Transfer

	No.	Technology title	WP7						WP8		WP9					WP10				WP11					WP12				
			UC_ADAS and C2X	UC_Highly automated driving	UC_Design and validation of next generation hybrid powertrain / E-Drive	UC_Modelling and functional safety analysis of an architecture for ACC system	UC_Infotainment and eCall Application Multi-Critical Application	UC_Next Generation Electronic Architecture for Commercial Vehicles	UC_Multi Domain Avionic Architecture	UC_Hybrid Avionics Integrated Architecture	UC_MPSoC Hardware for Space	UC_MPSoC Software and Tools for Space	UC_Optical Payload Applications	UC_Platform Applications	UC_Radar Payload Application	UC_Drives and electric motors in industrial applications	UC_Identification and authentication	UC_Tracking	UC_Manufacturing quality control by 3D inspection	UC_Multimedia communication WEBRTC	UC_Open deterministic networks	UC_Autonomic home networking	UC_Ultralowpower high datarate communi-cation	UC_Synchronized low-latency deterministic networks	UC_Seismic surveying by ship	UC_Video surveillance for critical infra-structure	UC_Medical imaging	UC_Control applications for critical infra-structure	UC_Railway applications
			T7.1	T7.2	T7.3	T7.4	T7.5	T7.6	T8.1	T8.2	T9.1	T9.2	T9.3	T9.4	T9.5	T10.1	T10.2	T10.3	T10.4	T11.1	T11.2	T11.3	T11.4	T11.5	T12.1	T12.2	T12.3	T12.4	T12.5
WP4	4.1	Heterogenous Multiprocessor SoC architectures (T4.1)	2					2			2		1				4												
	4.2	Dynamic reconfiguration on HW accelerators and reconfigurable logic (T4.2)			1						1			1															
	4.3	Networking (T4.3)	2		1												4					3	3			2			
	4.4	Verification and Validation Techniques (T4.4)			1						3						4												

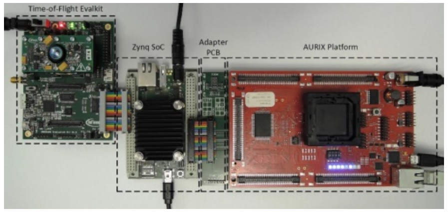
Technology transfer phases	
Definition	(red)
Evaluation	(orange)
Development	(yellow)
In Transfer	(light green)
Transfer complete	(green)

Scope 1: Complete implementation into use cases in the project
Scope 2: Partial implementation into use case
Scope 3: Will be transferred to LL (WP7-12) but not implemented into use case
Scope 4: Topic for future applications; technology transfer subsequent to EMC2

WP4 Achievements per technology

USPs/Highlights of WP4

- Architecture and Hardware support for mixed-criticality applications on multi-core platform along the 5 technology lanes
    - EMC2-DP platform – *Reconfiguration (T4.4)*



    - Software Defined **Asymmetric Multiprocessing** on EMC2-DP ZYNQ platform – *Architecture(T4.2)*
    - Heterogeneous TTNoC many-core architecture – *Networking (T4.3)*
    - High-Accurate Distributed Control Systems – *Networking (T4.3)*

    - **Analog-Mixed-Signal Power System** for MC Multi-Core - *Architecture*

- System optimisation for MCMC applications
    - **Time-of-Flight 3D Imaging** – *Application & Demonstration (T4.6)*
    - Application-specific Exploration and Optimization MCMC Hardware with **Virtual Hardware platform** – *Virtualization*

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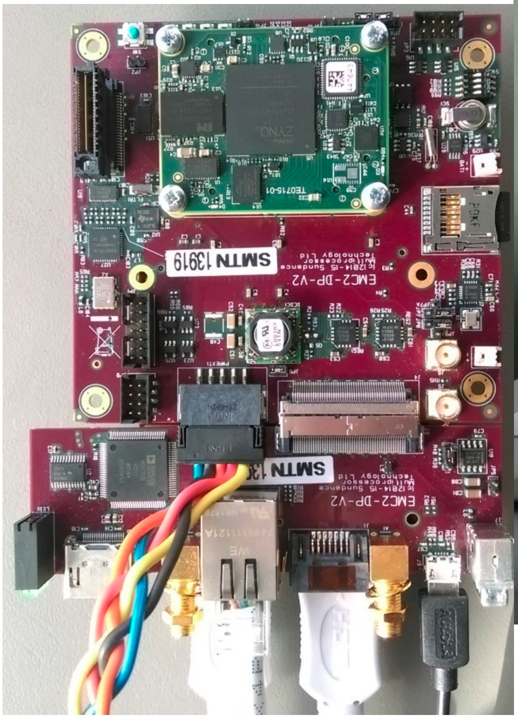
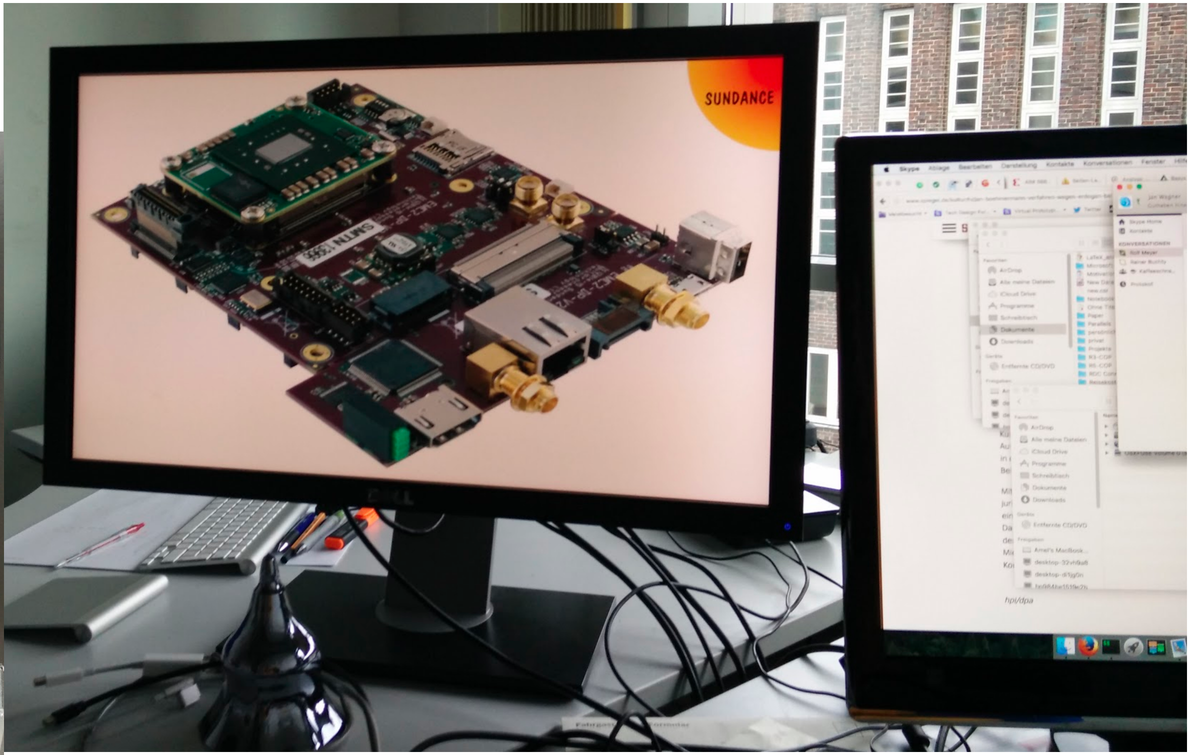
Highlights: T4.6

EMC2-DP, Zynq Base board: HDMI in and out, Ethernet, PCIexpress, SATA



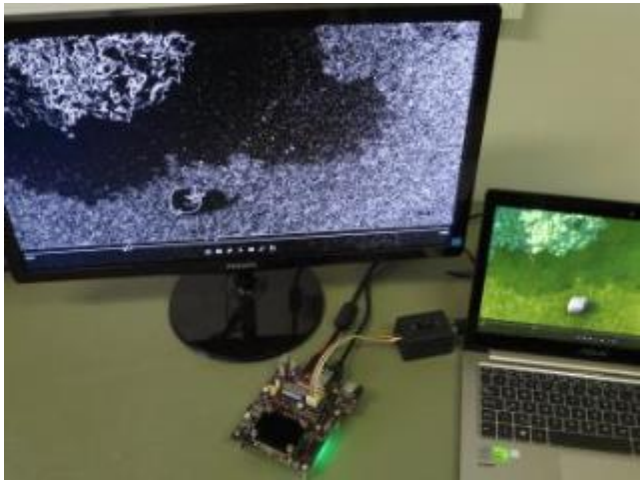


Highlights: T4.4/T4.6

Software Defined Asymmetric Multiprocessing on EMC2-DP ZYNQ platform

- EMC2-DP is Sundance HW platform enabling to use System on Module Component with ZYNQ.
- EMC2-DP is compatible with the Xilinx Software Defined System on Chip (SDSoC 2015.4) flow. UTIA & Sundance designed support for SDSoC.
- EMC2-DP parameters: MicroBlaze and UTIA EdkDSP floating point accelerator deliver:
  - Adaptive LMS filter: 776 MFLOP/s
- This is 2.3x faster than 666 MHz ARM A9 CPU optimized SW with NEON vector proc. unit.
- EMC2-DP HW image processing accelerators are generated by the SDSoC from C.
  See figure: Edge detection on Full HD Video:
  - EMC2-DP ARM + SDSoC HW: 60.0 Frames/s
  - EMC2-DP ARM + platform SW: 5.3 Frames/s

EMC2-DP



Demonstration

Demonstrators

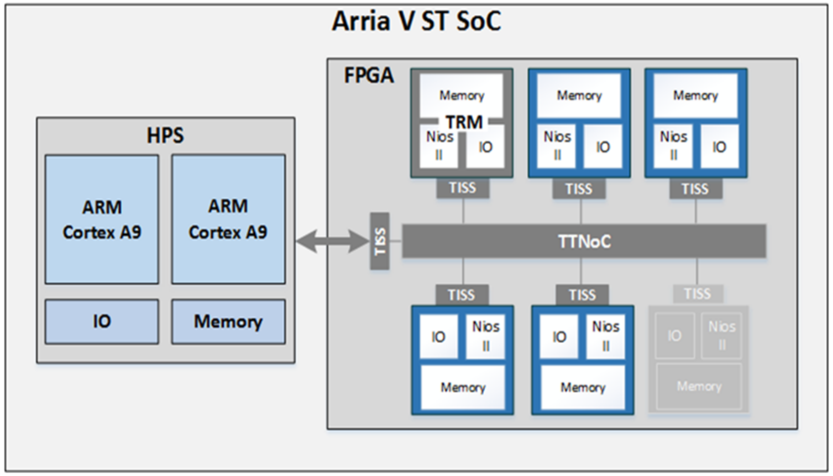
Object detection by HLS on EMC2-DP ZYNQ platform

- **Objectives**:
  - WP12.2 (LL6) is using the EMC2-DP is used for one solution to their object detection problem.
  - The idea is to use the FPGA for a object detection, but generate the FPGA code via high-level synthesis.
- **One solution of multiple prototypes**

Highlights: T4.3

Heterogeneous TTNoC many-core architecture (TU Wien)

- Objective: Building a deterministic heterogeneous architecture on Altera Arria V SoC
- Key achievements:
  - Integration of TTNoC on the Arria V SoC platform.
  - The architecture combines 4 Nios 2 components and an ARM Cortex A9 component.
  - Full time and space isolation of individual components, designed for mixed-criticality applications.



Block diagram of the architecture

Highlights: T4.3/T4.6

High-Accurate Distributed Control Systems (SevenS)

- Development of new White Rabbit nodes for the project to improve scalability and stability of the distributed frequency:
  - White Rabbit ZEN
  - White Rabbit LEN
- In terms of time in distributed networks considered as critical data, we have adapted White-Rabbit (able to provide time with <1ns accuracy) and also using our own devices, two distribute time over 14 hops maintaining synchronization capabilities with a jitter in 1-PPS signal under 250ps
- A new clock distribution mechanism (Peer-to-Peer and PeerDelay) to provide White-Rabbit with the possibility of being adapted to industrial Ethernet networks, which opens doors to the development of redundancy protocols such as High-availability Seamless Redundancy (HSR).

WR-ZEN

WR-LEN

Demonstrators

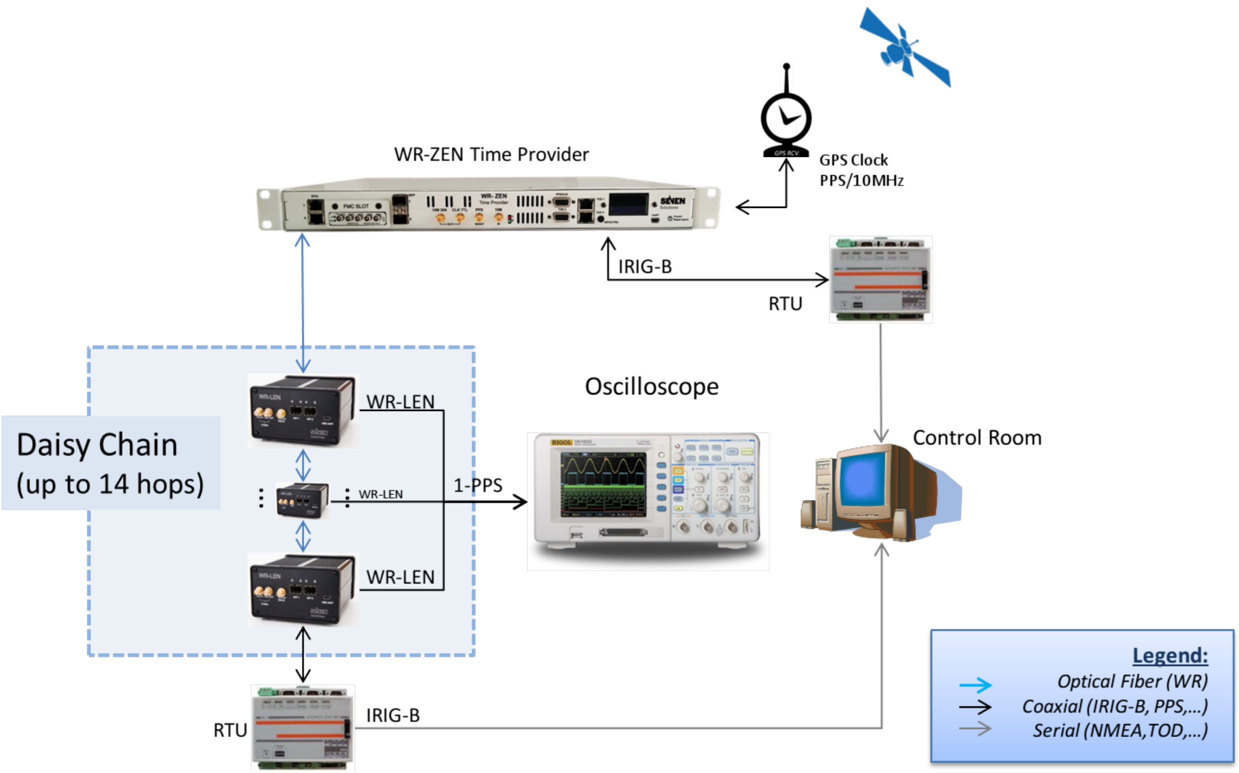
High-Accurate Distributed Control Systems (SevenS)

- **Objectives**:
  - Improvement of the synchronization performance in terms of jitter and skew of the distributed signal and the scalability of the timing network (WP4)
  - Implementation of redundant protocols (WP1) using new mechanisms to distribute time which includes the development of transparent clocks (WP4) (better synchronization, more scalable)
- **Two Prototypes**

Prototype A: <1ns accuracy deterministic time distribution system

Main features:

- **WR-ZEN** board as main time provider (better oscillator)
- **WR-LEN**, a double-port WR node
- **Accuracy <1ns** synchronization
- 1 Pulse per Second and 10MHz outputs
- Daisy-chain configurations with less than **250ps of jitter**
- **Scalable up to 12 nodes** in cascade
- Time distribution using **WR-PTP and IRIG-B**.
- Remote Time Units (RTU) connected to WR devices using IRIG-B



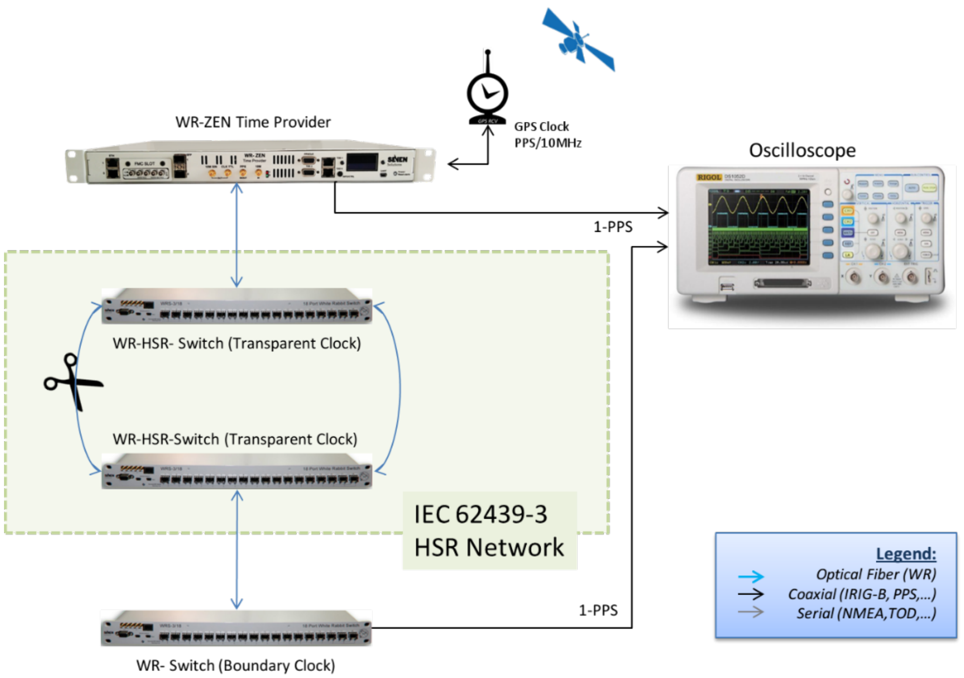
Prototype A

- Setup to demonstrate the scalability of the timing solution and also the utilization of different timing protocols in the same network.

Prototype B: Single point of failure avoidance using Transparent Clocks (Redundancy Protocols)

Main features:

- <1ns synchronization
- 1 Pulse per Second (1-PPS) and 10MHz outputs
- **Redundancy Capabilities** (HSR implementation for timing)
- Able to **recover** from a link failure **in ~zero-time**.
- 1-PPS skew improvement in terms of **~50ps**

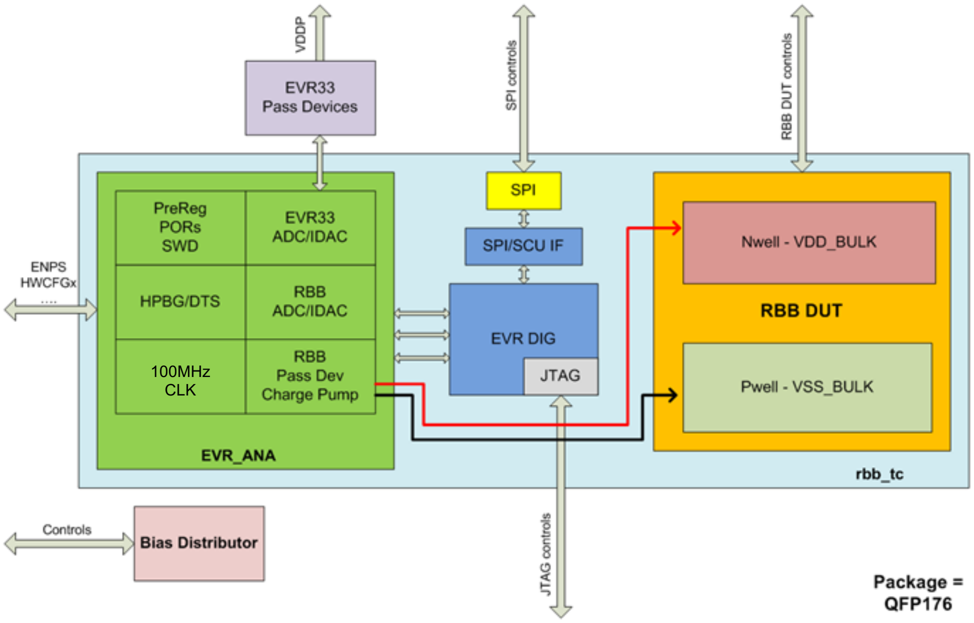


Prototype B

- Implementation of the HSR redundancy protocol using Transparent Clocks to recover from a system failure in ~zero-time.
- Demo will consist in how two devices connected to a HSR ring are able to remain 1-ns synchronized even after the main time reference is lost (link down).

Analog-Mixed-Signal Power System (Infineon)

- First full functional safety compliant Analog-Mixed-Signal Power System for multi core and mixed critical systems including standby controller, robust concept implementation, out of operating range functionality is now fully available for next generation of products.
- It introduce highest flexibility and have very efficient regulators with SMPS power optimization features, revers back biasing and dynamic voltage scaling.



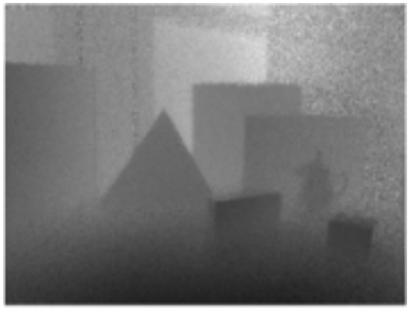
Block diagram of the concept

Highlights: T4.6

Time-of-Flight 3D Imaging (Infineon)

- Objective: Exploration of novel Time-of-Flight 3D imaging concepts targeting multi-cores and mixed-criticality
- Key achievements
  - ToF / RGB sensor fusion
    - First time high-performance sensor fusion solution for mobile devices achieved
    - Upscaled resolution, increased sharpness, less noise, less motion artifacts, high FPS
  - HW-accel. ToF processing
    - Novel Zynq-based system solution for mixed-critical app.

ToF 3D camera



Low-res. ToF image

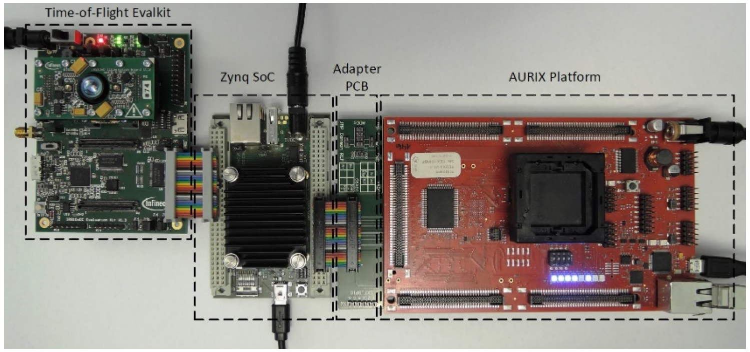
High-res. RGB image

ToF/RGB fused 3D image

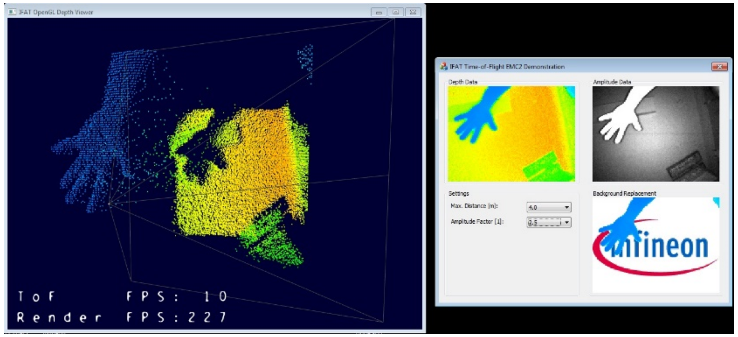
Demonstrators

Time-of-Flight 3D Imaging (Infineon)

- **Objective**: Exploration of novel Time-of-Flight 3D imaging concepts targeting multi-cores and mixed-criticality
- Setup
  - ToF / RGB sensor
  - Zynq platform
  - Aurix
  - PC

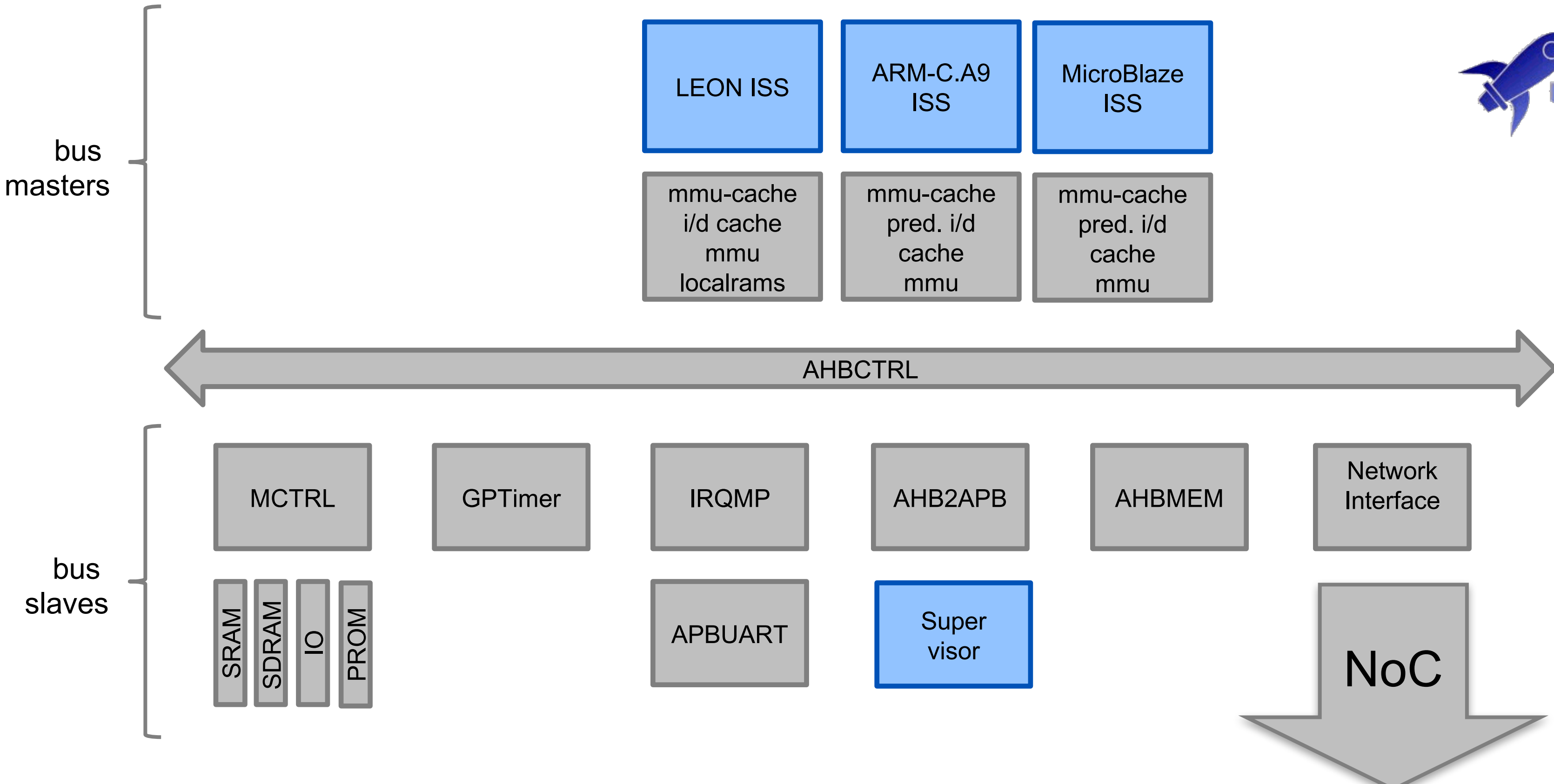


Hardware Setup



Example

Highlights: T4.6



All models available in loosely timed (LT), and approximately timed (AT) flavor of TLM2.0.

Implemented models

Demonstrators

Fault tolerant Heterogeneous Multi Processor Quadcopter Simulation WP2/WP4

- **Objectives**:
  - Provide an open mixed critical use application.
  - Simulate a fault tolerant motor control
    - 3 subsystems with different architectures
    - executing 3 different algorithms
    - One hardware voter
- **Work In Progress**
- **The design is build to be used with the EMC2-DP**

Possible configuration