Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments

EMC² Activity

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General Information

EMC² - Workshop on Embedded MultiCore systems for Mixed Criticality applications

Albert Cohen, INRIA

A half-day workshop was organized by ***EMC²*** at the HiPEAC Conference in Amsterdam, on January 20th, 2015. It was one of the largest workshops associated with HiPEAC, with 83 registered participants.

The focus was on concrete use cases of mixed-criticality, multicore applications, with invited presentations from project partners. A short overview of the project was given by the coordinator, Werner Weber from Infineon. Frank Oppenheimer from OFFIS (Germany) surveyed the architectures and tools of the project, and Sergio Saez from ITI (Spain) highlighted an innovative methodology and flow for tool integration. The program included applications from several domains that can profit from integration on a single chip. Together with the applications, their specific requirements including certification, performance and possible ways of integration will be presented. The workshop discussed possibilities of including dynamic aspects in addition to mixed-criticality on multicores.

Through productive interactions between speakers and the audience, the workshop acknowledged that embedded multicore applications increasingly integrate multiple functionalities on a single chip. Different domains evolve at different speed, depending on the certification processes and requirements; but most probably, these applications will show different criticality levels. Without significant changes and progress on the methodologies and tools, this will lead to a significant and potentially unacceptable increase of engineering and certification costs. Several approaches to keep these costs on a reasonable level follow the idea of partitioning in time and space and are already in the research pipeline. In order to develop reasonable approaches that allow the integration of different types of mixed-criticality application on a single system, the workshop clearly showed the value of examining concrete applications and requirements. Overall, the workshop was highly successful in disseminating ***EMC²*** results and collecting valuable insights from the computing systems community at large.

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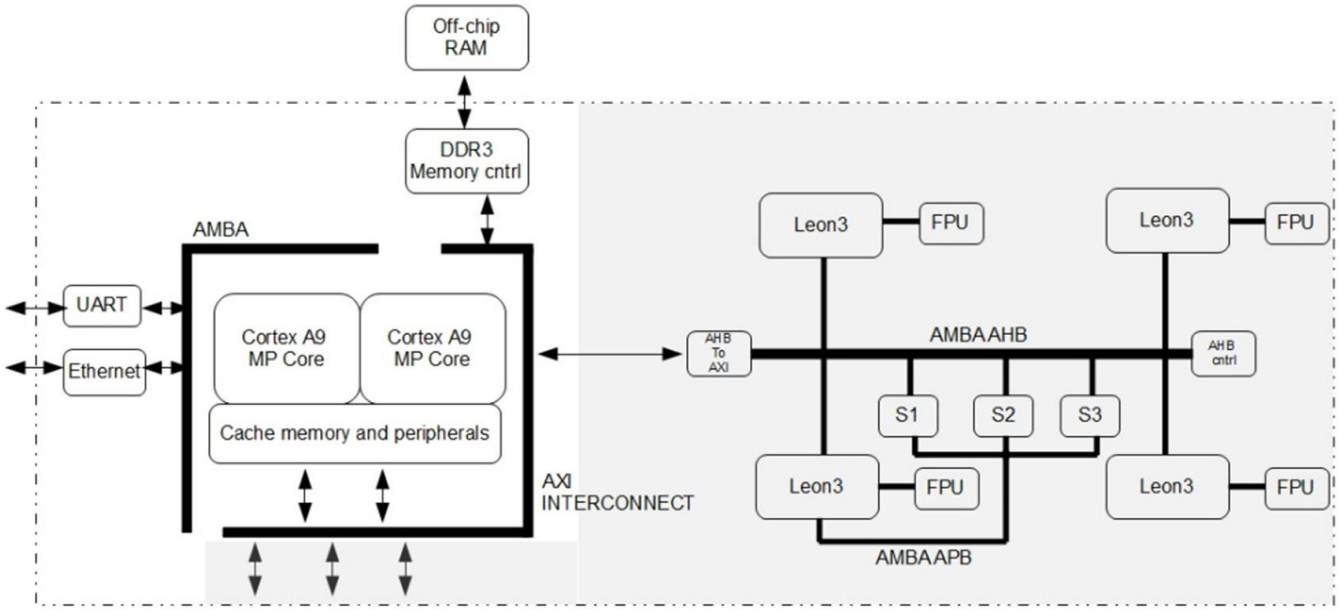
Heterogeneous multi-core AMP platform for embedded applications

Fabio Federici, Luigi Pomante, Giacomo Valente, Vittoriano Muttillo, Andrea Moro (UNIVAQ/DEWS)

In recent years, Field Programmable Gate Arrays (FPGAs) manufactures introduced new family of hybrid System-on-Chip devices, including advanced

processing units, hardwired peripheral subsystems and configurable logic blocks. Xilinx Zynq-7000 All Programmable system-on-chip, Altera Cyclone V SoC and Arria V SoC, and MicroSemi SmartFusion are notable example of such tendency.

whereas on ARM side an Ethernet controller and a UART controller will be connected. The four-core Leon3 will run a custom SMP-aware Linux distribution. The dual-core ARM will run a Linux Operating system and will offer a support for applications,



Xilinx Zynq-7000 is a family of configurable system on chip, including a hardwired dual-core ARM Cortex A9 processing unit (PS, processing system) and a configurable logic system (PL, programmable logic system) based on FPGA technology.

These platforms are particularly suitable for the implementation and verification of embedded systems based on multi-core processing architectures. In this regard, a platform for the evaluation of heterogeneous multiprocessor systems is currently under development. The system targets Xilinx Zynq7000 System on a Chip as primary implementation platform. Proposed system implements a multi-processor architecture based on the dual-core ARM Cortex A9 PS and a quad-core Leon3 processing subsystem implemented on the PL side.

The two subsystems are able to communicate via a shared, off-chip RAM memory. On the FPGA side, each Leon3 has a dedicated Floating Point Unit, able to take input data from Ethernet controller and UART controller, and to send this data toward the four-cores Leon3 by means of a shared mechanism built in off-chip RAM memory.

A working porting of the OpenMP library will be included on Leon3 side, fully supporting the execution of OpenMP based applications. Moreover, a hardware profiling system, currently under development, will be included in the Leon3-based subsystem. This will allow an accurate monitoring of the runtime behavior of the system, avoiding software execution overhead.

A localization application for wireless sensor networks will be considered as a benchmark to evaluate the performance of the system. The ZedBoard, an open evaluation and development board based on the Xilinx Zynq-7000 Configurable SoC, has been selected as the primary development platform for the proposed system.

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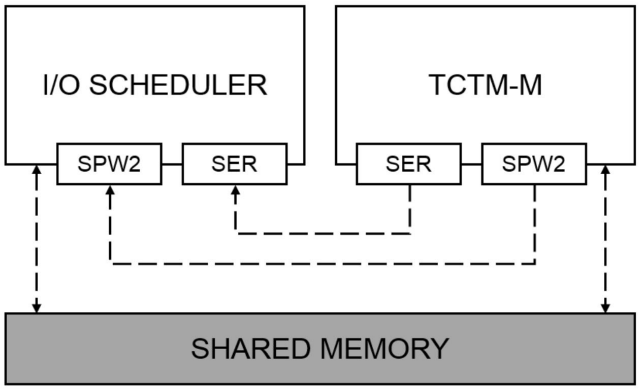
Safe and secure avionics multi-core platforms via paravirtualization

Dante Casalena, Fabio Federici, Luigi Pomante, Giacomo Valente (UNIVAQ/DEWS)
Danilo Andreetti, Dario Pascucci (TASI)

In recent years, there has been a growing interest towards multi-core and many-core architectures. Multi-core and many-core devices provide high computational capacity per footprint and allow a substantial reduction of energy consumption. However, they have the disadvantage of being less predictable with respect to single core architectures, given the heavy use of shared resources by the various processing elements. This is especially problematic in the avionics domain, where isolation and predictability are key requirements.



Virtualization appears as a very promising technique for implementing a robust software architecture for a multi-core system. By exploiting virtualization, multiple operating systems can run on top of a hypervisor able to manage the access to hardware resources. If the system includes hardware-based virtualization support, operating systems are able to run without any software modification. If not, it will be necessary to modify the operating system in order to run it on top of the hypervisor (paravirtualization). There are various examples of hypervisors specifically targeting aerospace and avionic domain. For example, the European Space Agency (ESA) promoted the development of XtratuM, AIR-II and PikeOS hypervisors.

In order to assess the effectiveness and performance of paravirtualization tools in relation to the specific requirements of a multi-processor platform specifically designed for the aerospace domain, a prototype platform is currently under development. The platform is based on a multi-processor system containing four Leon 4 microprocessors; two different hypervisors, XtratuM and PikeOS, have been considered.

An application simulating a satellite telemetry management system has been considered as a benchmark for the evaluation of proposed platform performances. An implementation of the application based on PikeOS hypervisor is currently under analysis. In the current state of the work, the architecture includes two partitions: an I/O Scheduler Partition and a Telemetry-Manager Partition. The I/O Scheduler Partition collects the I/O requests from the various applications, whereas the Telemetry Manager Partition is in charge to process and forward telemetry data. The two partitions communicate through shared memory and dedicated communication ports.

Preliminary tests have shown that the subdivision of the application between the two distinct PikeOS partitions makes possible the effective isolation in access to resources, thus justifying more effort on such a direction. Proposed platform will be further extended in the near future, also implementing the XtratuM-based version of proposed test application and carefully assessing the performance of the system in relation to specific requirements of the avionics domain.

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"Does it work? Mostly."

Andrei Terechko, Martijn Rutten (Vector Fabrics)

1 INTRODUCTION

In SP2 of the ***EMC²*** project Vector Fabrics (17H) has been developing dynamic program analysis to find costly bugs in embedded software. This work has resulted in a tool prototype Pareon Verify, which is now being productized by applying to application software from LL6. This article outlines the challenge of detecting dynamic issues in embedded software and builds up the case for dynamic program analysis tools. If you want your dynamic software to work always instead of mostly, contact sales@vectorfabrics.com for early access to Pareon Verify.

2 MULTICORE SOFTWARE DEFECTS

Today's software is inherently dynamic: reacting to external events, processing varying data, dynamically allocating memory. Bugs relating to the dynamic behavior are notoriously hard to detect. Once a bug triggers, finding the root cause often takes weeks of developer time. The costs? $2 billion Toyota field recall due to a "software glitch". The actual data from the VDC Research's 2010 Embedded Engineering Survey indicates that:

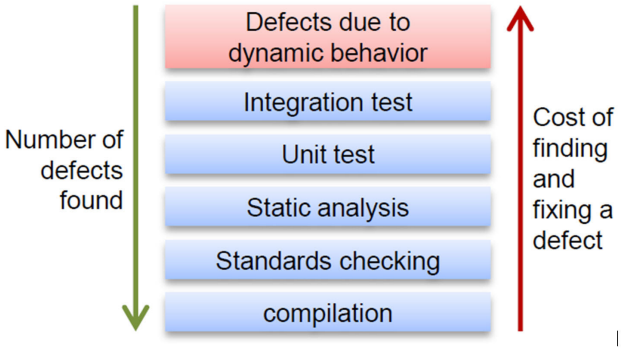
"The average total cost of software development for multicore/processor projects has risen to over 4.5 times the cost of projects that are using single processor architectures".

Multi-threading and parallel processing on new dual- and quad-core platforms makes the behavior even more dynamic. This leads to timing-related defects such as data races and deadlocks. As it is infeasible to verify all possible timing variations, many of these defects will only be found in the field by the end customer. Then what if a data race caused a glitch in the car's brake software? In his paper on "benign" data races the chairman of the ISO C++ Concurrency Study Group, Hans-J. Boehm shows that:

> "... all kinds of C or C++ source-level "benign" races discussed in the literature can in fact lead to incorrect execution as a result of perfectly reasonable compiler transformations, or when the program is moved to a different hardware platform".

3 SOFTWARE VERIFICATION THROUGH DYNAMIC ANALYSIS

Static analysis tools check against standards such as MISRA C and report issues in the static code structure. Even with 100% line code coverage from tests, defects in the dynamic behavior of the software slip through. Going up in the stack of test tools and methods, fewer defects are found. Yet the incurred cost of a defect goes up exponentially.



Dynamic program analysis (also referred to as Runtime Analysis) focuses on the behavior of the software. By actually executing the code, they get a global view on data and control flow. Avoiding the guesswork on how the software executes also means you do not get false positives. This is the missing link: detect the costly bugs that existing tools and methods fail to catch. Pareon Verify is a dynamic analysis technology that detects many of the top issues in the Common Weakness Enumeration (CWE). The tool can even detect buffer overflows when variables point into wrong, yet correctly allocated memory. Portability and scalability are known challenges that prohibit

practical use of dynamic analysis tools on embedded platforms. Pareon Verify is especially good on embedded platforms: it handles millions of lines of code and has no fundamental restrictions on the platform. Today, Pareon Verify supports 32-bit and 64-bit platforms, based on ARM and Intel/AMD processors and Linux or Android operating systems. Vector Fabrics is working hard to extend Pareon to other embedded platforms and operating systems.

Contact sales@vectorfabrics.com for support on your platform.

Contact: andrei@vectorfabrics.com

EMC²-Development Platform™

Flemming Christensen, Sundance Multiprocessor Technology Ltd.

Overview:

The ***EMC²***-DP™ is a PCIe/104 OneBank™ ARM+FPGA board that can be stacked with other boards to provide CPU Host Processing or dedicated I/O functions. The default version of the ***EMC²***-DP is using the Xilinx Zynq Z7015 FPGA with integrated Dual-Core FPGA, but can also be populated with other "System-on-Module" solutions, conforming to the 4x5 form-factor. The ***EMC²***-DP will integrate into Sundance's "Blades-for-PC/104" of stackable enclosures to build scalable solutions for ANY Embedded Solution.

The ***EMC²***-DP discounted with 50% to ***EMC²*** Universities Partners (€650.00) and 30% to ***EMC²*** Industrial Partners (€900.00) and is shipping in April of 2015

Key Features:

- PCIe/104 OneBank™ Carrier Board
  - 96mm x 90mm without I/O Expansion board
  - Compatible with stackable PC/104® concept
- Populate with Trenz 4x5 SoM Module Format

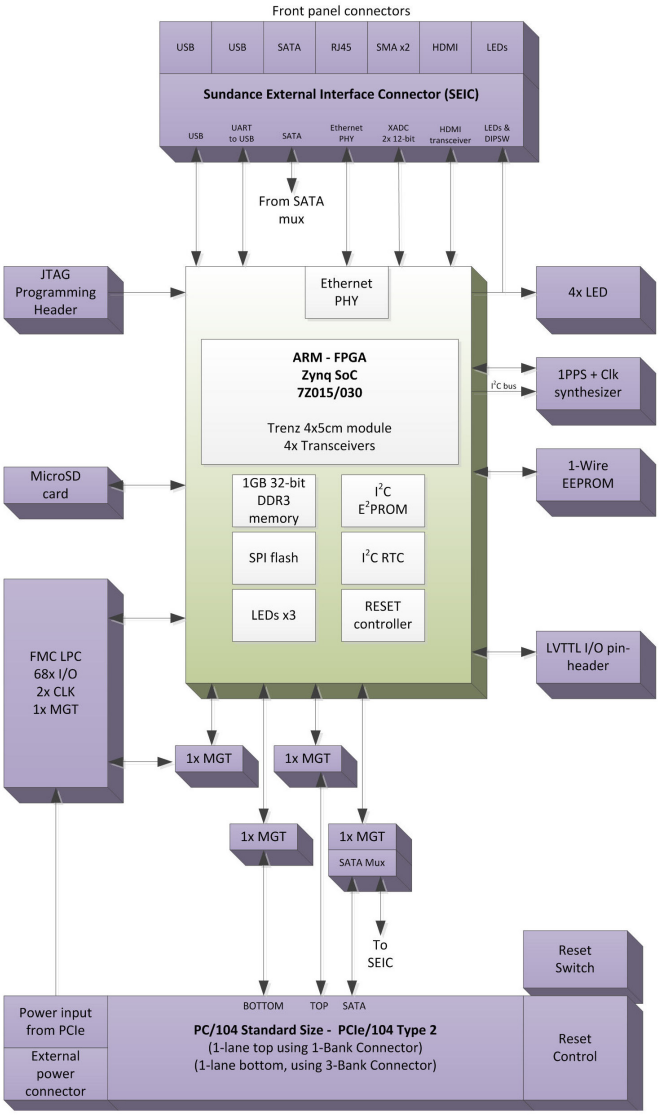


Figure 1 Block Diagram of EMC2-DP

  - Samtec® LSHM 2.5 mm shielded connectors
  - 260x I/O pins in three ruggedized sockets
- Fully compatible with TE0715 and TE0730
  - 1x Gen2 PCI-Express Lane on top stack
  - 1x Gen2 PCI-Express Lane on bottom stack
  - 1x SATA Interface on bottom stack/external
- Fully Compatible with VITA57.1 FMC-LPC™
  - 1x MGT Serial Link to VITA57.1 FMC-LPC™
  - 68x I/O on the VITA57.1 FMC-LPC™

- 1 pps on-board Clock synthesizer

• MicroSD slot for Booting of Linux

• 5VDC In or 12VDC Input Power

• Detachable 'Break-Out' I/O Board
  - 4-layer PCB for 'bespoke' custom design
  - Use 100x LSHM connector, as on SoM
  - Cable is an option for 'Custom' box's

*Figure 2 **EMC²**-DP Integrated*

in Blade for PC/104

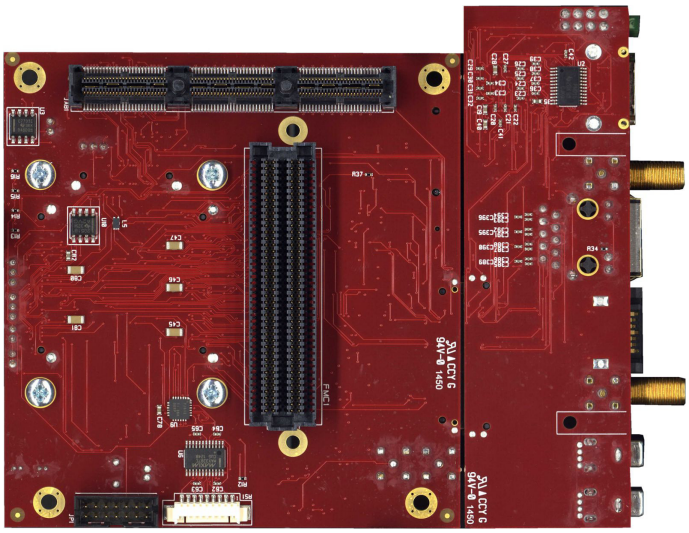


*Figure 3 1:1 Bottom of **EMC²**-DP, showing the FMC connector and the position of the FMC Module*

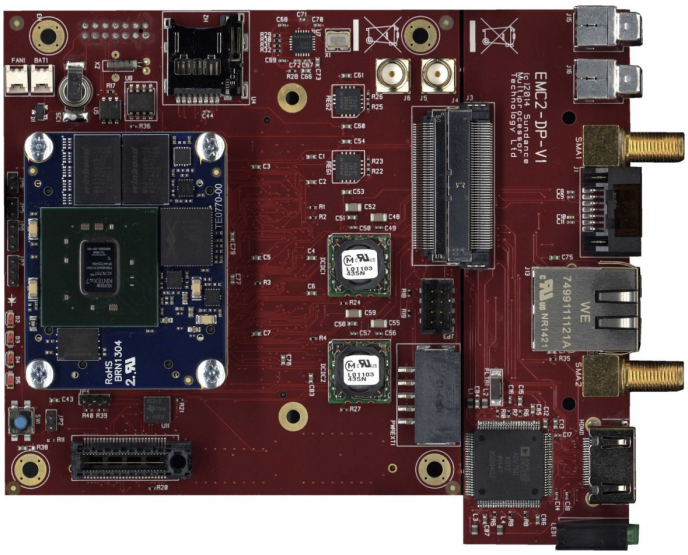


*Figure 4 1:1 Top of **EMC²**-DP, showing the SoM and the Sundance External Interface Connector (SEIC)*

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European Mixed-Criticality Cluster

MIXED-CRITICALITY CLUSTER
Contrex DREAMS PROXIMA

Kim Grüttner, Frank Oppenheimer (OFFIS)

Modern embedded applications already integrate a multitude of functionalities with potentially different criticality levels into a single system and this trend is expected to grow in the near future. Without appropriate preconditions, the integration of mixed-criticality subsystems can lead to a significant and potentially unacceptable increase of engineering and certification costs.

In many domains such as automotive, avionics and industrial control, the economic success depends on the ability to design, implement, qualify and certify advanced real-time embedded systems within bounded effort and costs. In those application domains there is also a trend toward an integrated approach under which different functions, possibly attributed to dif-

ferent criticality levels, share the same hardware, and therefore enable the standardization and modular encapsulation of service interfaces.

The integration of multiple functions with different criticality and certification assurance levels on a shared computing platform constitutes a mixed-criticality system (MCS). Mixed-criticality systems range from lowest assurance requirements up to the highest criticality levels (e.g., DAL A in RTCA DO-178B or SIL4 in EN ISO/IEC 61508 and ISO 26162).

The usage of multi-core processors is promising for many reasons: Reduction of installation space and weight due to the integration of multiple functionalities that have been deployed to multiple single-core processor before. Increase in dependability through multiple redundant execution of the same functionality. Implementation of new computation intensive application that could not be realized with previous available single processing performance.

These advantages come at the price of many challenges to be solved: The predictability of execution times cannot always be guaranteed due to unswayable-shared resource arbitration of shared caches and on chip interconnect (e.g. shared buses, crossbars with slave side arbitration or Network on Chips).
Since multi-cores Systems-on-Chips (SoCs) are highly integrated, using essentially the same silicon process technology, hardware errors and aging effects can have an influence on multiple functionalities. At the same time extra-functional parasitical effects, such as power and temperature need to be reconsidered to guarantee the functional and extra-functional integrity. Finally yet importantly, there is only little experience with the certification of multi-core systems available, which is currently mostly limited to dual-core systems.
For future utilization of multi- and many-core SoCs for mixed-criticality systems, the three integrated European research projects DREAMS [1], PROXIMA [2] and CONTREX [3] have joined their forces in the European Mixed-Criticality Cluster. To address the above-mentioned challenges, the cluster is addressing the following topics: combination of software virtualization and hardware segregation and the extension of partitioning mechanisms jointly addressing significant extra-functional requirements (e.g., time, energy and power budgets, adaptivity, reliability, safety, security, volume, weight, etc.) along with development and certification methodology. Furthermore, the European Mixed-Criticality Cluster will support the European Commission in the development of a joint Roadmap for mixed-criticality systems.

Recently started, and currently under construction, the www.mixedcriticalityforum.org website aims in establishing a joint forum for all projects, industrial, research and individual partners working in the area of mixed-criticality systems. It also will facilitate all interested parties to support the roadmapping process. The website has been officially announced and introduced during the MCS – "Integration of mixed-criticality subsystems on multi-core and many-core processors" workshop on January 19th 2015 at the HiPEAC conference in Amsterdam (https://www.hipeac.org/events/activities/7161/mcs/)

More information about the European Mixed-Criticality Cluster can be found in:
Salvador Trujillo, Roman Obermaisser, Kim Grüttner, Francisco J. Cazorla, Jon Perez. European Project Cluster on Mixed-Criticality Systems, In 3PMCES workshop - Performance, Power and Predictability of Many-Core Embedded Systems, Dresden, March 2014, http://tinyurl.com/mcc-paper

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Frank Oppenheimer (frank.oppenheimer@offis.de)

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1. http://www.dreams-project.eu/
2. http://www.proxima-project.eu/
3. https://contrex.offis.de

ARTEMIS project MBAT - Combined Model-based static Analysis and dynamic Testing of Embedded Systems

Erwin Schoitsch (AIT)

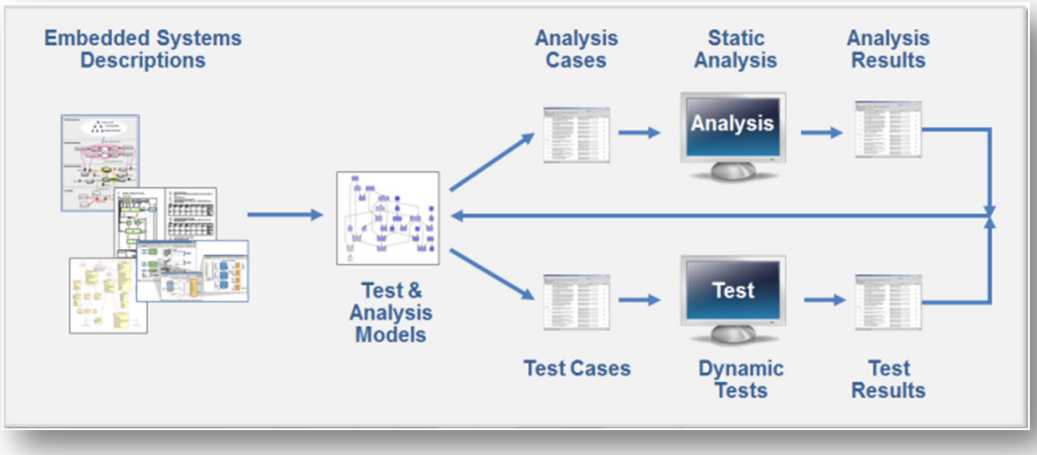


Figure 1: MBAT Concept: Combined Analysis and Test

MBAT was a project of the ARTEMIS Call 2010, funded by the ARTEMIS Joint Undertaking under grant agreement n° 269335 and the national funding authorities respectively the national public authorities of the 39 partners (from eight countries). The project was coordinated by Daimler (DE), project coordinator was Jens Herrmann, project manager was Michael Siegel from OFFIS (DE). The project started Nov. 1st, 2011 and finished Dec. 31st, 2014.
The research project targets the production of high-quality and safe embedded systems in a cost reducing way, with focus on the transportation domain(s) and testing. Domains covered have been automotive (including construction equipment/trucks), aerospace and railways.

MBAT aimed at achieving better results by combining test and analysis methods (Figure 1). A new leading-edge Reference Technology Platform (RTP) for effective and cost-reducing validation and verification of Embedded Systems was developed. This is of high value for the European industry and future projects, and contributes to the overarching ARTEMIS Goal of a Common Technology Reference Platform (CTRP). Therefore close co-operation with related projects was envisaged, especially with those of the ARTEMIS Safety & High-reliability Cluster (e.g. CESAR, MBAT, SafeCer, iFEST, VeTess, and continuing in CRYSTAL and ***EMC²***). MBAT was successful in particularly driving forward the so-called IOS (Interoperability Specification), based on OSLC (Open Services for Lifecycle Collaboration) which is standardized in an OASIS group (Open Advanced Standards for the Information Society, an non-profit industrial standardization consortium) for OSLC.

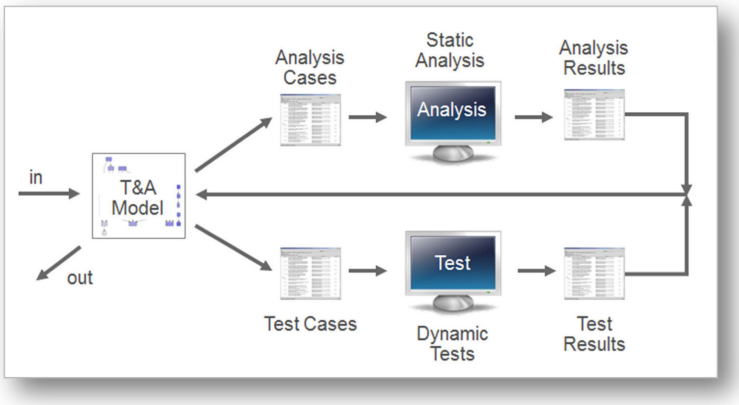
MBAT was an industrial use-case driven project. Besides management, exploitation, dissemination and standardization, three subprojects focused on the three major aspects of MBAT:

- SP1: Industrial Impacts (incl. particularly the use cases)
- SP2: MBAT Technologies & Innovations
- SP3: MBAT Reference Technology Platform

SP1 - Use Cases:
MBAT applied its technologies and innovations in 20 use cases in the three domains.The use cases were selected in such a manner that both, static analysis and dynamic test, had to be applied.

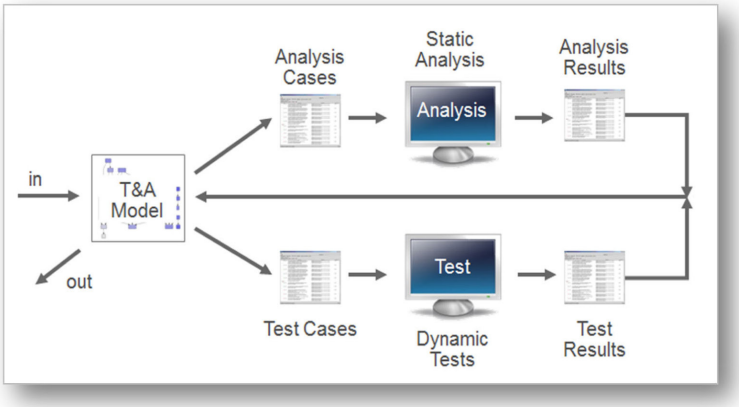
SP2 - MBAT Technologies & Innovations:
The MBAT technological approach can be best characterized by a layer concept: From Workflow via Patterns to Tool chains (see Figure 2):

Common Workflow Layer



Abstract MBAT Work Flow, many flows are possible

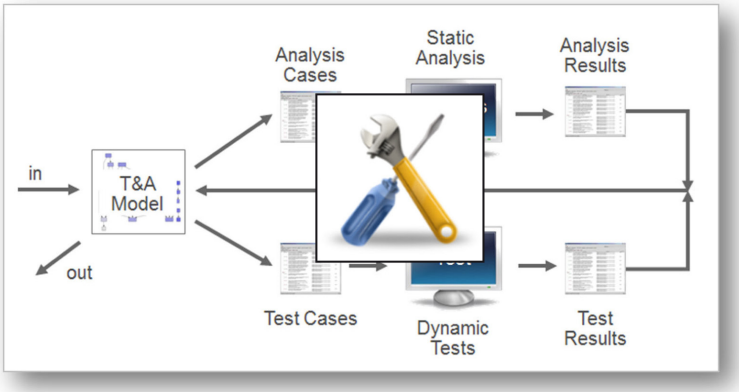
Method Layer



Apply MBAT A&T Patterns as e.g.

- first uncover all boundary value errors statically , then test the remaining cases
- first detect static flaws, then concentrate on testing these flaws

Tool Layer



Use MBAT A&T Tool Chains as e.g. Astree → Embedded Tester → PROVEtech:TA
(see also https://www.mbat-artemis.eu/joomla/index.php/downloads/category/10-public-deliverables)

Figure 2: From Workflow via Patterns to Tool Chains

MBAT developed a large collection of advanced techniques and tools for model-based analysis, test generation and execution made interoperable via a reference tool platform. However, a collection of individual tools is insufficient to achieve their full potentials in quality improvement and cost reduction. A main outcome of MBAT is a general methodology that supports an effective application and combination of the advanced model-based techniques for analysis, test case generation and test execution developed in MBAT. An overall approach has been developed

that uses iterative V&V planning as a backbone for dividing work into analysis and test activities and exploiting analysis and test results into an optimized V&V workflow.

On top of this was developed a pattern system for describing workflows that demonstrates how analysis and testing may be best applied. "A (solution) pattern is a (generic) solution for a certain problem in a given context".

Thus, it is not a finished solution that can be transformed directly into a running system, but it is a principal description or template for how to solve a recurring problem. A good pattern can be used in many different situations and defines a formalized best practice.

A pattern is described through a template that includes descriptions of the purpose of the pattern, when it is applicable, the participants, and the core workflow structure, etc. The workflow is described graphically using standardized notations like Business Process Model and Notation (BPMN) or UML Activity Diagrams.

An instance (or known-use) of the pattern defines the exact set of tools used to support the workflow activities of the pattern and the exact artefacts exchanged among them. An example is provided in Figure 4.

The MBAT project has developed more than 18 patterns covering most levels of system V&V ranging from requirements formalization to runtime monitoring. Lately, the pattern collection has been reorganized and provided by an online wiki-based

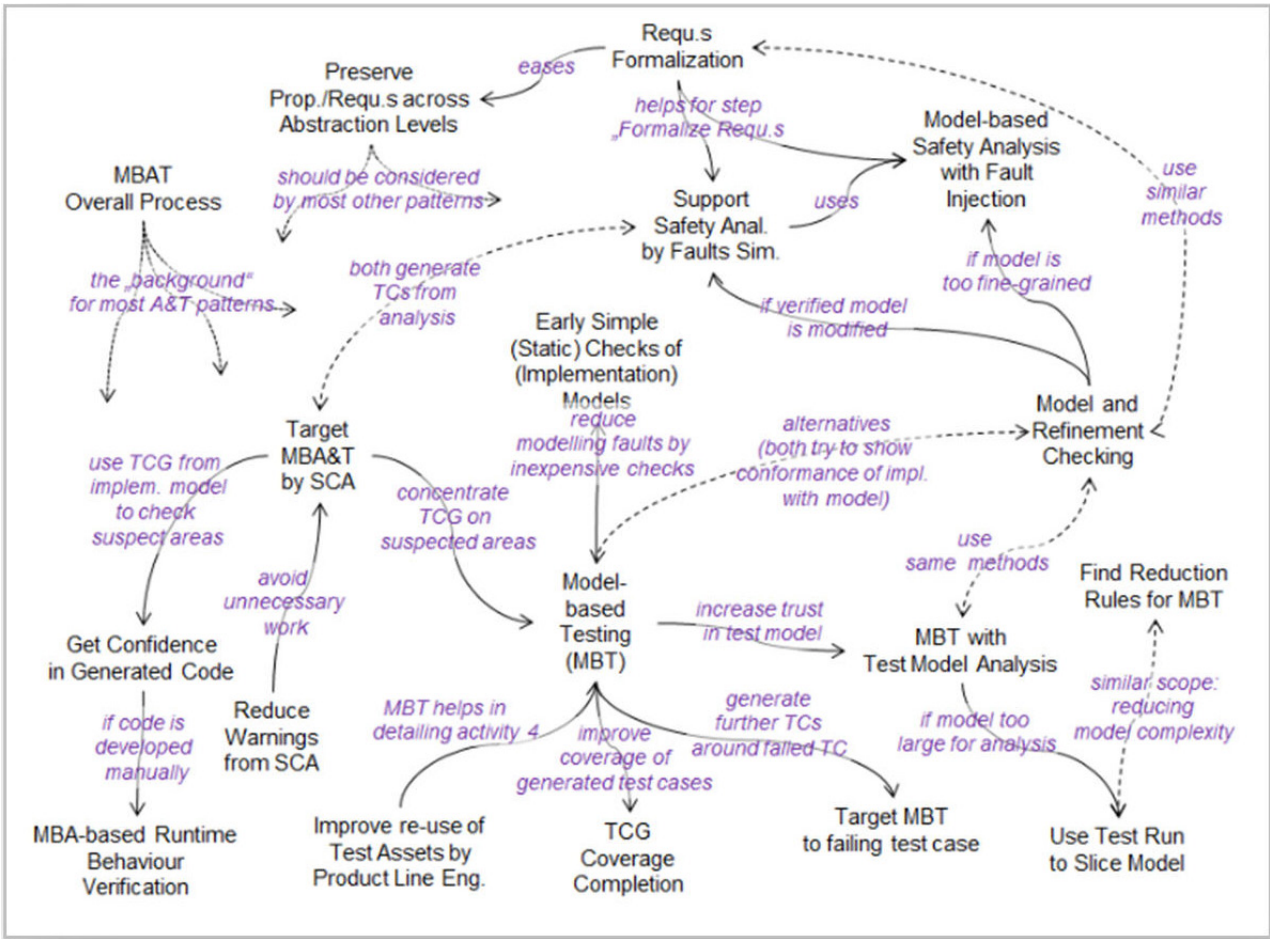


Figure 3: MBAT Analysis & Test (A & T) Patterns

system (http://mbat-wiki.iese.fraunhofer.de). Additional information is available on the MBAT public website www.mbat-artemis.eu, Public Deliverables. One example is explained in some detail here:
Overview of the MBAT A&T Pattern System (Analysis & Test):

Figure 3 gives a brief overview of the MBAT patterns that have been identified and elaborated during the course of MBAT. The figure below shows these patterns (i.e. their names) as well as main relationships between them (there are actually more relationships listed in the pattern descriptions, but showing all would render the diagram confusing). Solid lines indicate supporting relationships, while dashed lines indicate similarities.

Additional detailed explanations are available on https://www.mbatartemis.eu/joomla/index.php/downloads/category/10-public-deliverables , particularly in the "Experience Package", final edition.
An example for a MBAT-pattern:
MBAT Overall Process - Pattern

Also Known As: (MBAT's) Combined Model-based Analysis and Test Approach

Origin: Jens Hermann (DAI) – Technical Annex, fig. 2, Brian Nielsen (AAU) – update for 2nd project review
Purpose: The „meta-pattern" of the MBAT methodology. In principle, all other AT-patterns are related to this pattern.

Context/Pre-Conditions:
Critical system development, where several analysis and test methods/tools are already used, but with either too high costs or insufficient quality or efficiency.
To consider: tools from different sources usually speak different languages; hence their useful combination needs good guidance (enforcing tool combination at any cost likely fails).
Structure:

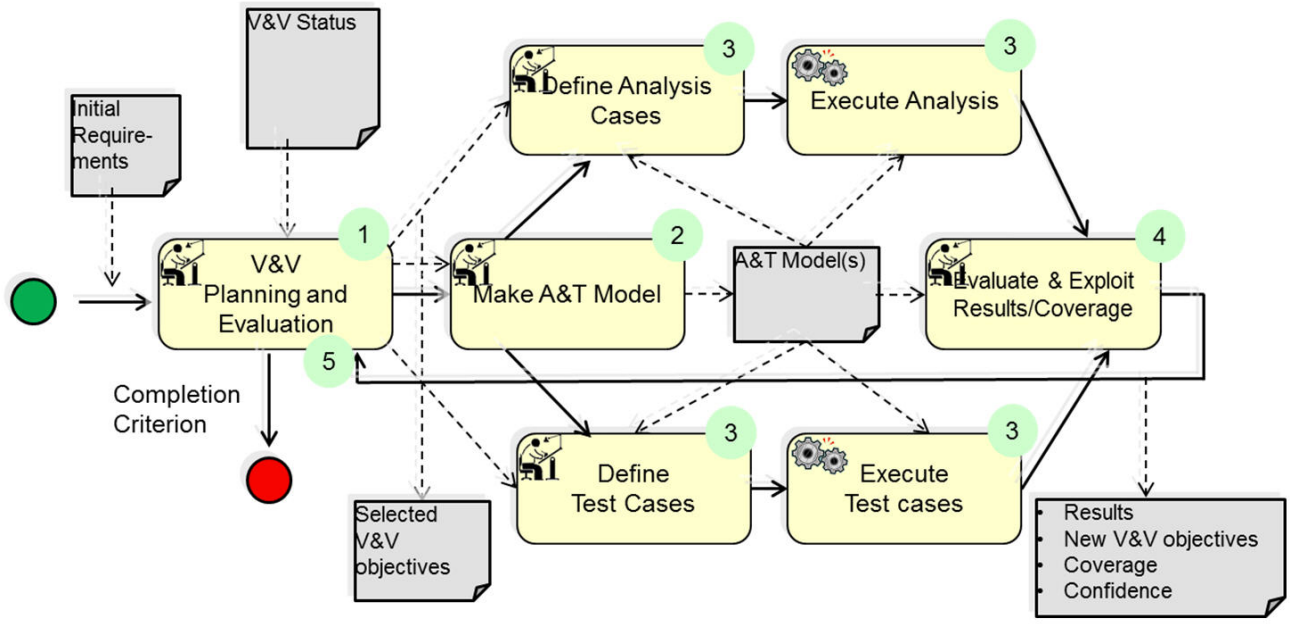


Figure 4: Structure of "MBAT Overall Process"

Participants:

• Req(uirements): those properties, for which the fulfilment by the target system has to be shown with the combined analysis and test methods. Requirements can be functional or non-functional. If the system needs V&V at several levels (e.g. model, component, code), requirements for a certain level can be derived from objectives of the higher level, and itself define the objectives for the next lower level.

• V&V Plan & Status: documentation that assigns V&V steps (analysis or test) with requirements, and V&V steps with tools. This may occur hierarchically. It may define a V&V flow, and collects V&V results traceable.

• A&T Model(s): artefact(s) that describe(s) relevant system properties at a level of abstraction appropriate for the application of A&T tools.

• Analysis case: a particular static analysis step

• Test case: a particular dynamic test step

Critical Requirements Bin: Example Assessment Matrix								
Rqmt	Ver*	Val**	DT	OT	Techniques	Scheduling	Resources	
Assess 1	X							
a					code analysis	start + 3 months	code analysis software	
Assess 2	X	X						
b					audit	start + 4 months	software engineers	
d					audit	start + 5 months	software engineers	
Assess 3		X	X					
c					doctrine review	start + 3 months	doctrine, military reviewer	
d					audit	start + 5 months	software engineers	
e					system integration	start + 6 months	computer engineers	
Assess 4		X		X				

Actions/Collaborations:

1. The V&V plan is established by deciding for each requirement how it's fulfilment can be shown best. For that purpose, an appropriate combination of analysis or test methods is chosen. If this is not possible due to the requirement's complexity, it is restructured into more detailed requirements, for which this step is repeated.
2. A&T models are prepared. This can be achieved using various sources and techniques, from manual creation to automatic derivation, e.g. from requirements. Validation of models should be considered, in particular if generated manually.
3. A&T steps are executed, presumably after some preparation and usually according to a given workflow. They use the A&T models and provide results, which are recorded with the V&V plan.
4. The outcomes are inspected and evaluated.
5. Depending on these results, the V&V plan, the A&T model(s), and even requirements may require a modification, and a subsequent optimizing A or T step may be initiated exploiting the results from the current step.

Notes:

• Steps 3 and 4 are repeated until all requirements are fulfilled or a violation is encountered that enforces a modification of the SUT.

• If a requirement violation exhibits incorrect requirements, these are corrected and the process continued.

• Steps 1 and 2 have no strict order.

Known Uses: all MBAT use cases apply the MBAT overall process

Related Patterns: in various ways, all A&T patterns are related, typically as sub-patterns.

SP3 – MBAT Reference Technology Platform

This subproject covered the contribution of MBAT to the overarching ARTEMIS goal of the High-Reliability Cluster of projects mentioned before to a Collaborative Reference Technology Platform. This platform is not a "tool-chain" for all applications nor domains but rather a collection of tools which can be combined to a domain or application specific tool chain by using the so-called IOS (Interoperability Specification) for system engineering based on OSLC (see Figure 6).

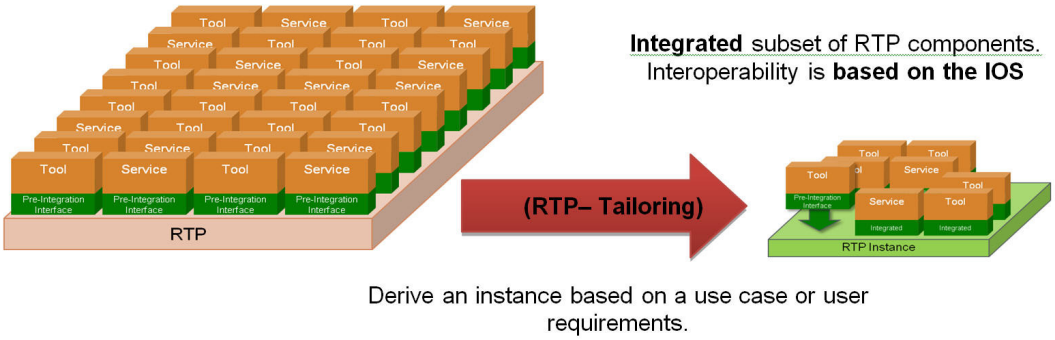


Figure 5: CRTP as a set of tools and services to be tailored for an application or domain

The concept was developed in the ARTEMIS project CESAR and is after MBAT now further developed in the ARTEMIS project CRYSTAL and will be supported towards a harmonized standard in the Innovation Action CP-SETIS, a support-action type H2020 project).

Establishing a common Reference Technology Platform enables co-operation between developers, bridging the gap between different development tools chains and integrating development artefacts of different engineering domains (see Figure 10).

MBAT has implemented a Task Force focused on the MBAT IOS to coordinate pre-standardization activities within the project in order to reach a consensus on common specifications to be disseminated beyond it and to initiate concrete cross-project collaborations within the ARTEMIS eco-system, notably with CRYSTAL, for paving the way towards pre-standardization of sustainable Interoperability Specifications at a larger scale in Europe.

It is worth noting that interactions have been successfully initiated and will be followed up with the OSLC community, notably with contributors of the OSLC Configuration Management specifications being under elaboration within the OASIS standardization consortium. But it is well known that standardization takes longer than the duration of a research project and can only take up results of the project which are of a certain maturity to be achieved only towards the end of the project.

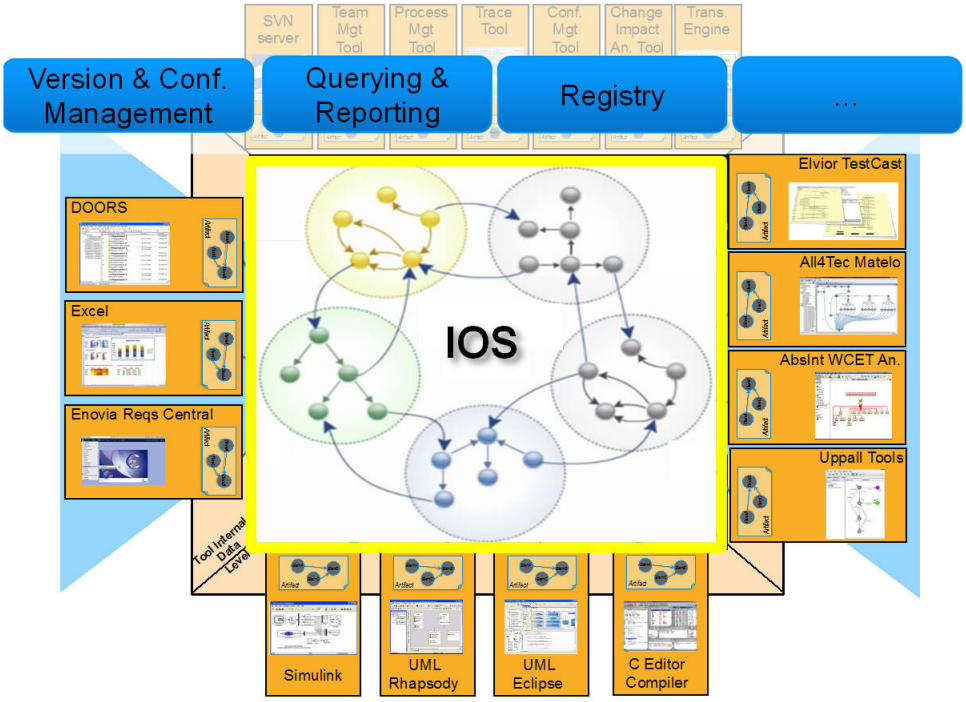


Figure 6: Schematic overview of MBAT IOS

MBAT Overall Results:

The paragraph provides a short overview of the results and impact of MBAT in a concise manner from industries point of view, showing that the initial goals and ARTEMIS goals have been successfully achieved:

- 17 A&T Method Patterns and supporting Tool Chains – all evaluated in 20 use cases (http://mbat-wiki.iese.fraunhofer.de/)
- Project has influenced technical standards as e.g.
  - UML Test Profile, which is under development by the OMG
  - the ARTEMIS Interoperability Specification (IOS) for the interaction of Embedded System Engineering Tools
- Project has influenced technical standards as e.g.
  - UML Test Profile, which is under development by the OMG
  - the ARTEMIS Interoperability Specification (IOS) for the interaction of Embedded System Engineering Tools
- Prepared further business by establishing new contacts for further collaboration on technical topics
- 100+ MBAT publications and public deliverables available, see www.mbat-artemis.eu and https://www.zotero.org/groups/mbatproject
- Shown in industrial use cases: using MBAT V&V technologies it is possible to
  - gain an increased V&V coverage of the embedded system under test by at least 20%
  - reduce costs for V&V by at least 15%

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Call for Papers

ERCIM/EWICS/ARTEMIS Workshop on "Dependable Embedded Cyber-physical Systems and Systems-of-Systems" at
SAFECOMP 2015 – Delft, Sept. 22 - 25, 2015,
Co-hosted by CP-SETIS and the ARTEMIS projects EMC^2, ARROWHEAD, CRYSTAL, nSafeCer

Since it was established in 1979 by the European Workshop on Industrial Computer Systems, Technical Committee 7 on Reliability, Safety and Security (EWICS TC7), SAFECOMP has contributed to the progress of the state-of-the-art in dependable application of computers in safety-related and safety-critical systems. SAFECOMP is an annual event covering the experience and new trends in the areas of safety, security and reliability of critical computer applications. It provides ample opportunity to exchange insights and experience on emerging methods, approaches and practical solutions.

The 34th edition of SAFECOMP (http://safecomp2015.tudelft.nl/) focuses on the challenges arising from networked multi-actor systems for delivery of mission-critical and safety critical services, including issues of the "Systems-of-Systems" area, cyber-security, medical technology and patient care.
The already well-established ERCIM/EWICS/ARTEMIS Workshop on Dependable Embedded Cyber-physical Systems and Systems-of-Systems" of the ERCIM DES-Working Group, is again taking place on the Workshop-Day Sept. 22, 2015!!
Sessions are planned on

- Dependable and resilient embedded systems,
- Highly automated (autonomous) Systems and Robotics,
- Systems - of- Cyber-Physical Systems,

and particularly addressing thematic topics such as

- Multi-core platforms and mixed criticality systems
- Safety and security co-engineering
- Standardization (interoperability, cyber-security aware safety) and certification

covering aspects from design, development, verification and validation, certification, maintenance, standardization and education & training. This is a workshop, and to be distinct from the SAFECOMP conference mainstream, it allows reports on on-going work aiming at hopefully fruitful discussions and experience exchange.

Reports on European or national research projects (as part of the required dissemination) as well as industrial experience reports from work in progress are welcome.
You want to present your ideas and results? What do you have to provide?
Workshop proceedings will be provided as complementary booklet to the SAFECOMP Proceedings in Springer LNCS. Please keep your paper format according to SPRINGER LNCS style guidelines (http://www.springer.com/computer/lncs?SGWID=0-164-6-793341-0) (use Microsoft Word if possible). Papers (8 - 12 pages) will be reviewed by at least three reviewers.

Deadlines:

- Full paper submission: 22 May 2015
- Notification of acceptance: 15 June 2015
- Camera-ready submission: 28 June 2015

The International Programme Committee is composed of selected EWICS and ERCIM members, led by the workshop organizers.

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Special Session on IEEE INDIN Conference, Cambridge, UK, June 22-24

EMC² recognizes that Cyber-physical systems (CPS) are the key innovation driver to improve almost all mechatronic products with cheaper and even new functionalities. Furthermore, they strongly support today's information society as inter-system communication enabler. Consequently boundaries of application domains are alleviated and ad-hoc connections and interoperability play an increasing role. At the same time, multi-core and many-core computing platforms are becoming available on the market and provide a breakthrough for system (and application) integration. A major industrial challenge arises facing (cost) efficient integration of different applications with different levels of safety and security on interconnected computing platforms in an open context.

After about 1 year of project lifetime, EMC²has already started producing tangible results. As such, it is time that EMC²project partners can bring their research results to the forefront of the international scientific community, exchange ideas with external audience and benefit from constructive discussions.
In this context, EMC² will be hosting a Special Session (SS) in the context of the forthcoming IEEE conference on Industrial Informatics (INDIN 2015), to be held on July 22 to 24, at Cambridge, UK (www.indin2015.org).

The special session will be on "Embedded Multi-Core Systems for Mixed Criticality Applications in Dynamic and Changeable Real-Time Environments" and it is co-organized by Dr. George Dimitrakopoulos (Asst. prof. Harokopio University of Athens, Greece), Dipl.-Ing. Erwin Schoitsch (Austrian Institute of Technology GmbH, Austria) and EMC² project manager Dr. Werner Weber (Infineon Technologies AG, Germany).
The session will include a high number of original research papers, emphasizing on project results, from joint efforts among industry and academia players, not only from project partners, but also from external participants. The topics that the papers will focus on, revolve around the following areas:

1. Architectures and platforms for embedded (cyber-physical) systems
2. Application Models and Design Tools for Mixed-Critical, Multi-Core CPS
3. Dynamic runtime environments and services
4. Multi-core hardware architectures and concepts
5. System design platform, tools, models and interoperability
6. Applications of multi-core cyber-physical systems: avionics, automotive, space, cross-domain and other applications
7. Safety and security co-engineering in open dynamic CPS
8. Next generation embedded/cyber-physical systems
9. Standardization, qualification and certification issues of complex critical CPS

IEEE INDIN constitutes a series of high prestige conferences, usually gaining attendance of high profile key industrial and research players. As such, it will be a great opportunity for enhancing extroversion actions for the project partners, who can disseminate their results to a large and demanding audience. Moreover, the event, will prepare partners for future research articles work that will further communicate the project's results in prestigious journals. Last, the discussions that will take place during the event are expected to pave the way for future research and commercial initiatives in the field of industrial informatics.

EMC² project partners are invited to participate in the conference, showing how interesting EMC² work is and how far we can get with it!

--
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Project:

EMC²-- Embedded Multi-Core systems for Mixed Criticality applications in dynamic and changeable real-time environments

ARTEMIS Grant Agreement Number: 621429

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